TECHNICAL UNIVERSITY OF LIBEREC
Faculty of Mechatronics, Informatics and Interdisciplinary Studies

Institute of Information Technology and Electronics

RELIABILITY ASSESSMENT AND ADVANCED MEASUREMENTS IN MODERN NANOSCALE FPGAS

Spolehlivost mikroelektronických obvodů a nanostruktur

Porovnání a zvyšování spolehlivosti číslicových aplikačně specifických a programovatelných integrovaných obvodů

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Abstract (EN)

The doctoral Ph.D. dissertation thesis (Thesis) deals with the study of possibilities to evaluate reliability of circuits based on modern nanostructures. It also presents a new way of measurement of various internal parameters of microelectronic circuits based on modern nanotechnologies. This thesis presents a new solution and methodology of utilization of BRAM in FPGA and utilization of this modern part in dependable systems, enabling a new easy way of implementation, reliability assessment methodology and measurements in modern nanoscale microelectronics, computer systems and architectures gaining from the amazing world of programmable technologies.

Keywords:

Microelectronics, nanotechnology, FPGA, BTI, BRAM, internal parameters, aging, reliability and dependable digital systems

Abstract (CZ)

Disertační práce se zabývá studiem možností stanovení určitých spolehlivostních parametrů moderních obvodů a nanostruktur. V této práci je prezentován nový způsob měření různých parametrů mikroelektronických obvodů moderních nanotechnologií. Zcela nové řešení a metodologie využívá BRAM bloků v programovatelných obvodech FPGA, jako běžnou součást moderních řešení použitých i v systémech se zvýšenou provozní spolehlivostí. Prezentované řešení je novou metodologií. Umožňuje nový jednoduchý způsob implementace, odhadu a stanovení spolehlivostních ukazatelů, včetně měření parametrů moderní mikro- a nanoelektroniky, počítačových systémů a architektur těžících z ohromujícího světa programovatelných technologií.

Klíčová slova:

Mikroelektronika, nanotechnologie, FPGA, BTI, BRAM, parametry a stárnutí obvodů, provozní spolehlivost a spolehlivé digitální systémy

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Contents

"Constant advances in manufacturing yield and field reliability are important enabling factors for electronic devices pervading our lives, from medical to consumer electronics, from railways to the automotive and avionics scenarios. At the same time, both technology and architectures are today at a turning point; many ideas are being proposed to postpone the end of Moore's law such as extending CMOS technology as well as finding alternatives to it like CNTFET, QCA, memristors, etc, while at the architectural level, the spin towards higher frequencies and aggressive dynamic instruction scheduling has been replaced by the trend of including many simpler cores on a single die. These paradigm shifts imply new dependability issues and thus require a rethinking of design, manufacturing, testing, and validation of reliable next-generation systems. These manufacturability and dependability issues will be resolved efficiently only if a cross-layer approach that takes into account technology, circuit and architectural aspects will be developed.",

from COST MEDIAN Action IC1103.

The speed of development and implementation of innovative technologies and introduction of advanced processes and methods is really extremely fast and amazing. Rapidly growing portfolio of new technologies in design and manufacturing of advanced integrated circuits allow higher integration of complex structures at ultra-high nano-scale densities. However, the new devices are sensitive to negative effects of various changes of the internal nanostructures and parameters. The extremely fast downscaling of the semiconductor technology makes reliability a first order concern in modern high-performance as well as large low-power designs. Most of the new technologies have introduced new faster or low-power circuits and solutions. However, they are very expensive and all the dramatically increasing complexity of the design and simulation phases, together with strong pressure towards shorter time-to-market intervals, makes any precise testing and research tasks of the new structures extremely difficult within the given time frames. In addition, the increased integration densities make the reliability of integrated circuits the most crucial point in modern advanced systems as well as in any dependable system. It also is the very important task to develop and validate advanced measurement and reliability assessment methods together or along with the new technologies, nanoscale integrated circuits and manufacturing processes.

Reliability physics, reliability issues, its assessment and the system dependability aspects are one of the key areas to be solved and the key points of huge investments today. Teams all around the globe work on many advanced solutions. I do propose a low-cost and fast "on-chip" method without utilization of expensive external measurement equipment. It is directly linked to the quality issues of the devices, allowing circuit parametric measurements. The proposed method and methodology allows variability and aging measurements fully on-chip, in addition, it creates the "holy-grail" of reliability measurements and also allows us to evaluate foundry technology directly on their product.

1 Introduction

Rapidly growing portfolio of new technologies in design and manufacturing of advanced integrated circuits allow higher integration of complex structures in ultra-high nano-scale densities. The speed of development and implementation of innovative technologies is amazing. FPGA (Field Programmable Gate Array) allow designing logic circuits directly in software. FPGAs consist of sets of high number of after-manufacturing custom configurable programmable circuits and memory block elements and units. In addition, FPGA devices are introduced very soon or just together with the new technologies used in ASIC (Application Specific Integrated Circuits). Today's technologies get closer and closer to the physical limits and the nature of physics. It also is one of the main reasons why the new devices are sensitive to negative effects of various changes of the internal nanostructures and parameters.

The process and parameter variability is increasing rapidly. The effects get much more visible on the latest generally available 28 nm, 22 nm (ready just now), or 14 to 16 nm technologies (under development or sampled in the first commercial lots nowadays) and their respective feature sizes. Voltage scaling does not keep pace with physical scaling and poses serious reliability issues like BTI (Bias Temperature Instability), HCI (Hot Carrier Injection), TDDB (Time-Dependant Dielectric Breakdown), etc. Higher current densities result in various electromigration effects. The aging of the electronic nanostructures, as well as the most of the generally negative internal changes due to various physical mechanisms, causes changes in parameters of CMOS structures; PMOS transistors are generally considered to be more sensitive than NMOS transistor structures. It is typically demonstrated as changes in the gate threshold levels. These changes also result in lowering of the maximal drain current as well as cut-off frequency, elongating the processing delays in the aging-affected circuits, compared to the original design. In case of dependable systems, the key parameter lies in the negative changes in delays of critical paths. The system failures due to such negative effects must be avoided. Hence, all the critical changes have to be detected, in the ideal case the given or sufficient time before it results in the system failure. The new FinFET technology offers many advantages over the traditional planar MOSFETs; however their reliability performance is still not fully understood. NBTI in planar PMOS as PBTI in NMOS has been considered as a less important threat in the earlier nodes having SiO_2/SiON gate oxides. With the introduction of HKMG (High-k Metal Gate), the gate leakage has been reduced, but it has become a serious reliability concern along with BTI-related issues.

Changes in parameters due to process variations and aging along the working lifetime, as well as power supply voltage and temperature variations, can result in significant signal delays and may affect the final design quality and dependability. Especially BTI-inducted delays and timing variations may result in delay faults, propagating up to the device or equipment malfunction or failure. In deep-submicrometer devices and nano-scale technologies, it is why NBTI (Negative Bias Temperature Instability), caused in PMOS transistor structures by long low signal levels at the gates, or PBTI (Positive BTI), similar effect observed also in NMOS FET structures when scaling the technology down, also RTN (Random Telegraph Noise) and many new phenomena became visible and important factors influencing circuit's and the chip reliability parameters or lifetime.

Reliability of electronics will be the main concern in future design and development of new microelectronics and nanotechnologies. Reliability physics, reliability issues, its assessment and the system dependability aspects are one of the key areas to be solved and the key point of huge investments and work today. Teams all around the globe work on many advanced solutions.

The thesis document presents an interesting new method, theory and results obtained in various tests including the important values of total delays or signal parametric changes. I do propose a new, low-cost and fast "on-chip" method without utilization of expensive external measurement equipment. It is directly linked to the quality issues of the devices, allowing circuit parametric measurements. The proposed method and methodology allows wide range of basic as well as aging measurements fully on-chip. It could create the “holy-grail” of reliability measurements and also allows us to evaluate foundry technology directly on their product. The aspects of overall power consumption and other factors and conditions are also discussed. There are many measurement results present in this document. In addition, the measurements were performed on different technology nodes, including the latest low-power ones. This document also investigates the area of various effects caused by the main stress factors values to the FPGA chip design and related design trade-offs.

1.1 Background

In 1975, Gordon Moore (born 1929 in San Francisco, California), co-founder of industry leader Intel Corporation, predicted that the number of transistors on a chip would double about every two years [*1*]. This is known as Moore’s law and it says that technology revolution as the number of transistors integrated into microprocessor chips has to be exponentially increased for greater computing power. More has also predicted some limits, however those were and are successfully beaten as many other limits predicted many times years ago. In 1971, the Intel 4004 4-bit processor contained 2300 transistors, manufactured using 10 µm process and on the die area of 12 mm^2 and running at 741 kHz with max. TDP 0,63W [*2*]. Since November 2011, the highest transistor count is in Intel's 61-core 244-thread Xeon Phi commercially available 64-bit CPU with over 5 billion transistors, manufactured using 22 nm 3-D tri-Gate transistor technology at the die area of about 700 mm^2 and it has Max. TDP of very high 300 W [*3*]. The product is codenamed Knights Landing using a 14nm process as it was announced in June 2013 [*4*]. The absolute record holds is probably held by NVIDIA Corporation with its Kepler GK110-based 7.1 billion transistor Super GPU, manufactured using TSMC’s 28 nm manufacturing process [*5*] with Max. TDP close to 300 W. In the world of programmable logic gates, the biggest chip today is Xilinx Virtex-7 2000T FPGA, which integrates 2 million logic cells providing an equivalent of 20 million ASIC gates and incorporating 6.8 billion transistors using Stacked Silicon Interconnect technology with 28 nm TSMC’s HPL [*6*] (low power with HKMG) die technology with 65 nm interposer and 19W max. TDP [*7*]. And the technology is moving forward extremely fast to 20 nm TSMC process generally available now for logic [*8*], Intel’s 14 nm technology for high-end processors [*9*], and many other technologies for memories from 14 nm to 20 nm technology nodes and feature size from other key technology leaders, like Samsung, IBM, or the newest 15 nm Toshiba NAND memories [*10*].

Reliability of semiconductor devices and dependability of electronics equipment is one of the most discussed topics today. Many hard-working teams and scientists try to solve really hot issues worldwide. Working in this area for many years, I have performed number of researches and literature search using IEEE, Google and other search engines and also my original programs and scripts running on public as well as non-public databases, where a costly membership is required and offering much more information for my work. Base on a general search in the key areas, Figure 1 shows really strong evolution of the number of IEEE publications from publishers IEEE, AIP, IET, AVS, MITP, VDE, Alcatel-Lucent, IBM, BIAI, TUP and Morgan & Claypool, including conference publications, journals and magazines, books and eBooks, Early Access Articles, standards, and education and learning materials from available files since 1965. Figure 2 show search results for the publications about FPGA

reliability. All the figures show strongly increasing number of published results or ideas, in fact doubled during the last 10 years. It is a clear evidence of very strong interest of research teams as well as development, manufacturing and also implicative interest of customers in work and results in these areas, as this documents aims at as well.

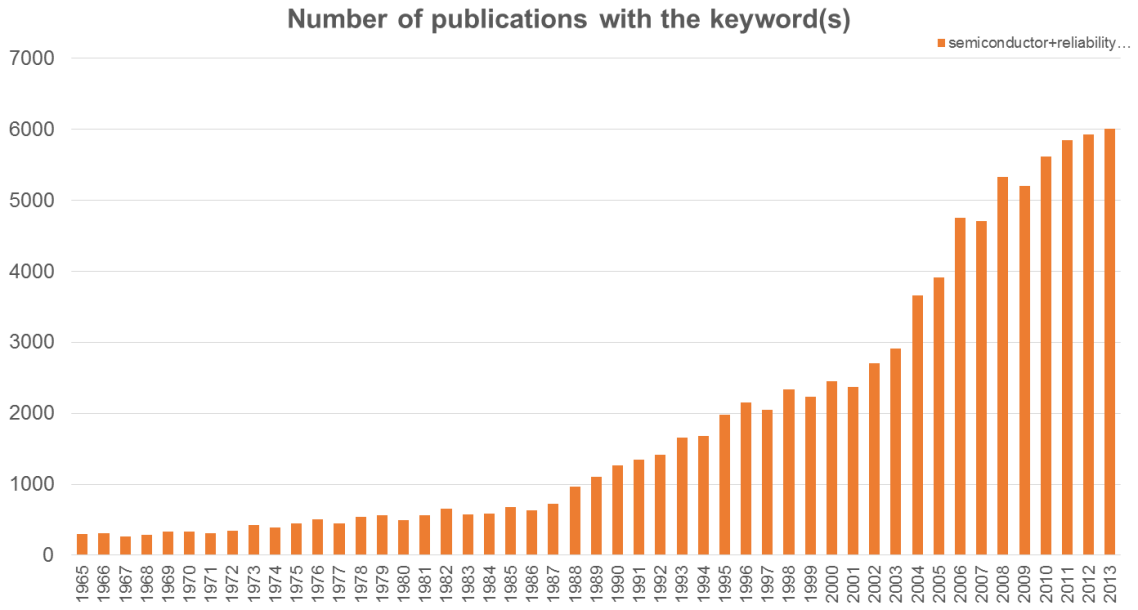

Figure 1. Evolution of the number of publications with keywords "semiconductor reliability".

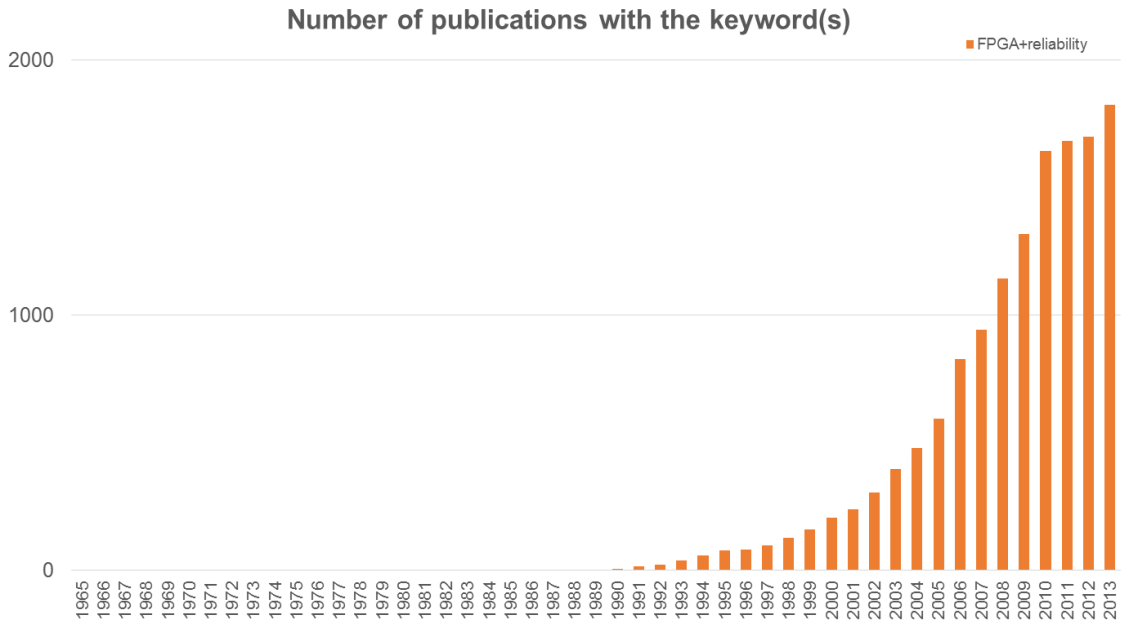

Figure 2. Evolution of the number of publications with keywords "FPGA reliability".

1.2 Motivation

The aggressive scaling of technologies requires utilization of new methods and materials. The nanoscale technologies and devices are subjects to various degradation processes. Application-specific integrated circuits (ASIC) allow design of special or support circuits, however such

products are very expensive in their design as well as manufacturing processes. Fortunately, the invention of programmable devices, especially the Field Programmable Gate Array (FPGA) and their programmable structures have already enabled wider changes in the application functions after its manufacture process. In addition, the most advanced programmable chips are introduced at the newest available and the smallest feature sizes, the minimum designed size of a transistor or a wire in either the *x* or *y* dimension, in very short time after the very first availability of new ASIC devices.

Parameters of devices and internal structures can be measured by external or internal circuits and methods. Today, BRAM (block random access memories) are a very standard part of FPGAs. However, **there is absolutely no any publication that discuss or deals with such a way of utilization of BRAMs** for measurements in the chips and also using such data and results for evaluation of the device reliability parameters in order to analyse the actual platform, its actual state and estimate the system dependability. Is possible to create and evaluate multiple programmable test structures, including the measurement blocks, directly on a Field-Programmable Gate Array (FPGA) chip? Is possible to perform a reliability assessment using Lab-On-Chip methodology and with BRAMs?

1.3 Structure of the Thesis

The thesis document has about 190 pages in total and it is organized into 7 comprehensive chapters as follows:

- ***Chapter 1 - Introduction*** - describes the motivation behind the work efforts together with the goals. There is also *Problem Statement subchapter* showing the problem statement, contribution and structure of this thesis, as well as a large list of the main contributions of this thesis.
- ***Chapter 2 State-of-the-art and Theoretical Framework*** – tries to make and overview of the area discussed further and describes the actual level of knowledge related to the problem stated in this document. It also describes the details of the methodology and related theories.
- ***Chapter 3 – Description of the New Method*** introduces the new method and describes its details.
- ***Chapter 4 – Experiment and results*** - presents a number of experiments, performed measurements and their results.
- ***Chapter 5 - Delay-Fault Run-Time XOR-less Aging Detection Unit Using BRAM in modern FPGAs*** – introduces my second and completely new method, it describes a completely new solution which can be combined with the new method in order to analyse complex systems with much lower overhead.
- ***Chapter 6 - Integration of the Solutions in Complex Systems*** – deals with implementation of the methodology and the solution in selected modern systems.
- ***Chapter 7 – Conclusions -*** makes an overview of this document, presented results, the contribution of the work itself, and it also deals with the future steps and possible further research work.
- References, Appendixes, Glossary and Index.

1.4 Problem Statement, Research Goals

This chapter contains a concise description of the main issues that need to be addressed before anyone tries to solve the problem. Here is list of the problems that the following my research should address:

- The measurement and evaluation processes used in microelectronics and also on modern chips and ASIC devices are very expensive. Most of the reliability-related issues and methods require extremely cost- and time-intensive equipment and approach. Is possible to perform at least some tasks a bit cheaper and also faster and using public, generally available tools?
- There is absolutely no any publication that discuss or deals with such a way of utilization of BRAMs for measurements in the chips and also using such data and results for evaluation of the device reliability parameters in order to analyse the actual platform, its actual state and estimate the system dependability.
- Is possible to create and evaluate multiple programmable test structures, including the measurement blocks, directly on a Field-Programmable Gate Array (FPGA) chip?
- Can BRAMs sustain the testability of chips (also very important topic discussed today)?
- Is possible to perform a reliability assessment using Lab-On-Chip methodology and with BRAMs?

How the new materials can impact it and what could be the evolution of the discussed areas?

1.5 Contributions of the Thesis

The thesis has to be a significant contribution to the area of modern measurement methods and it tries to introduce, map and analyse a completely new area of research. It introduces many completely new methods, ideas, ways of implementation and also important results, not generally available before. The work is focused on SRAM-type or rewritable configuration cell based FPGAs, however many of the ideas and method are applicable to many other systems and technologies.

The following new information is to be introduced by my work and in this document:

- a new method and implementation of measurement of basic parameters of internal structures using BRAM and modified ring oscillator circuits,
- a new differential method for aging measurement purposes using BRAM,
- many new results from measurements of sub-micrometre, deep sub-micrometre and emerging very deep sub-micrometre technologies, especially 45nm, 40 nm and 28 nm FPGAs and technologies,
- technology bottlenecks and important facts observed during set up or during measurements and experiments under extreme conditions,
- an unusual comparison of modern technologies,
- a number of new previously unpublished information and ideas.

2 State-of-the-art

The rapidly growing world of FPGA devices offers important as well as interesting platforms for analyses of process scaling. It also creates new study opportunities in process variations and degradation effects. Changes in parameters of FPGAs in time or under either power supply voltage or temperature variations result in timing variations or delays and may affect the final design quality and dependability. Such timing variations may result in delay faults, up to the final device or equipment malfunction or failure. Today, many dependable systems are based on programmable devices. Designs with programmable structures, such as FPGA devices, must be carefully simulated and tested during the design phase. This area is well-covered by many papers and publications and is being investigated again with the new processes and key technology nodes coming out every approximately 2 years.

Very interesting work and source is [*12*], where the authors published their wide work, which is close area to mine. There are also many other publications of this team from London available ([*13*], [*14*], [*15*], [*16*], etc.) , representing probably one of the top works in this area close to mine and also time. At that time (year 2011), I have developed similar solutions completely independently, my solutions use different circuits and I have been focused on new technologies. However it is nice to see similar independent approach, also validated by this as well as few other research teams.

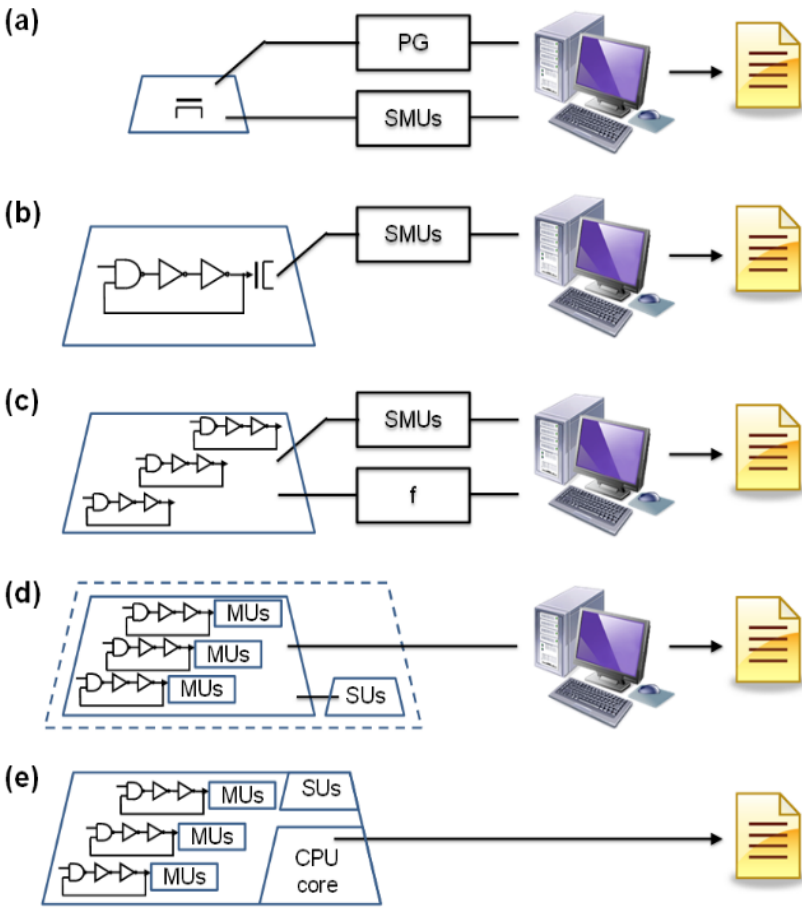

Figure 3. Evolution of technology reliability evaluation.

Legend: (a) Measurement of a single device under test with external instrumentation. (b) Signal generation on chip, measured with external instrumentation. (c) On-chip time-dependent variability measured with multiple on-chip circuits. (d) On-chip circuits and measurement instrumentation generated ad-hoc in advanced FPGAs, described in this work. (e) Near future: employing integrated processors for data analysis. *Note: This figure was created in cooperation with imec (B. Kaczer)*

The reliability of semiconductor devices and integrated circuits gets much more visible since 1960s, starting from works like [*17*] or [*18*] and [*19*], up to one of the latest papers [*20*] from the last year 2014. A great overview of the Design Tools for Reliability Analysis can be found in [*21*]. Ring Oscillator Reliability Model to Hardware Correlation in 45 nm SOI [*22*].

The work-horse approach of reliability qualification has always been stressing and measuring of individual devices, either at wafer or at package levels (Figure 3a). To surpass constrains imposed by contacts and cabling, some groups have integrated part of their external instrumentation,

such as GHz frequency sources, directly on chip (Figure 3b). Others have added multiple identical test structures, as well as on-chip selectors, allowing them to study time-dependent variability in deeply scaled technologies (Figure 3c). Using 28 nm technology Field-Programmable Gate Arrays, multiple test structures, including the measurement instrumentation, can be ad-hoc created and evaluated directly on the chip (Figure 3d). A concept of an entire "reliability lab-on-chip" is therefore demonstrated in the thesis document. This concept can also be further extended by employing for example the high-end FPGA embedded processor in the aging evaluation (Figure 3e) of the platform itself, also enabling a completely new dimension of self-intelligence in self-awareness systems.

Dependability is a measure of a system's availability, reliability, and its maintainability, standardized by a set of TC56 standards (IEC60050-191/2: Vocabulary, and so forth). It is also possible to find the following four dimensions of dependability - availability, reliability, safety and security. Dependability, or reliability, describes the ability of a system or component to function under stated conditions for a specified period of time. Dependability is also the most important system property for critical systems, where the costs of effects of the system or equipment failure may be very high. It is a case for example in safety-critical systems, mission-critical systems, or also many other critical systems, like financial or business-critical systems. It is obvious that dependability, and hence the reliability of all the key system components, has to be discussed and solicited in much more systems, than it could be observed years ago.

The reliability of a system can be defined as the ability to perform the specified function(s) under stated condition(s). Various approaches, difficulties, methods, e.g. exist. In general, mechanical reliability prediction is more difficult problem compared to pure electronics or software reliability. The so-called bath-tube curve represents the typical life cycle and device reliability phases of any device, circuit, equipment or part of it. The exact waveform varies case-to-case, however all devices displays 3 basic phases, as shows in the following figure. The reliability assessment works with the most stable and the most important part of the device lifetime – the useful time. It tries to evaluate the reliability parameters (like lambda) and to predict the length of the useful device life frame, estimate the point of end of time in the wear-out phase. It is generally considered to start at the point of the initial, post-manufacturing and post-burn-out phase, where devices are subjects to so-called initial or infant mortality. Figure 4 show how the bathtub curve changes with respect to the modern or latest technologies – the initial reliability is lower or infant mortality is higher, while the useful device life gets shorter and the failure rate during the wear out phase increases and the degradation of the device during this phase gets faster.

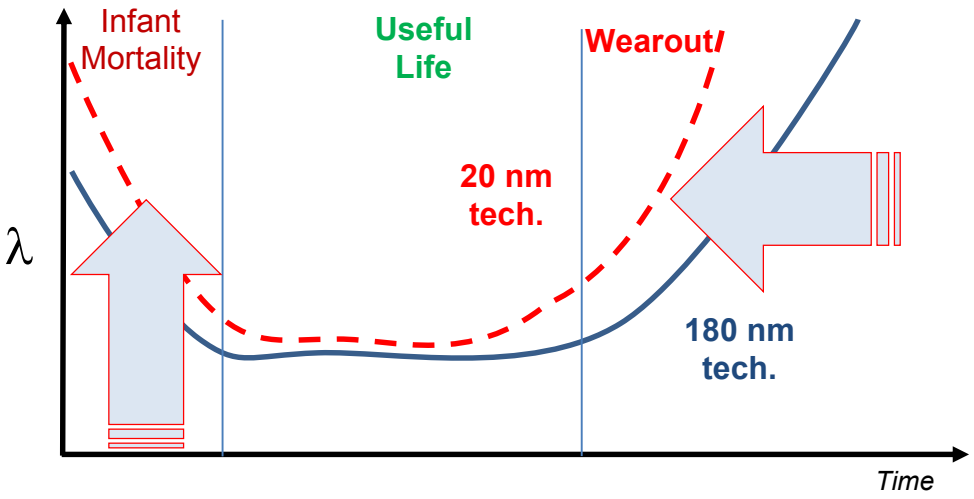

Figure 4. The bathtub curve with respect to the new modern technologies

The objective of a reliability prediction is to determine if the equipment design will have the ability to perform its required functions for the duration of a specified mission profile under given conditions or environment. Reliability predictions are usually given in terms of fails per million hour or mean time between failures (MTBF) or failures in time (FIT).

Mean time between failures (MTBF) is the predicted elapsed time between inherent failures of a system during operation, calculated typically as the arithmetic mean (average) time between failures of a system. It is also used and valid for repairable products. Some systems are not intended to be repaired (non-repairable products, excluding production phase), hence mean time to failure (MTTF) is used in this case, which measures average time to failures with the modelling assumption that the failed system is not repaired. Hence it is very important to perform a classification of the work and repair conditions, device or component lifetime, failures, modes and repair actions. It has direct impact to the way and evaluation of the reliability parameters and reliability assessment itself.

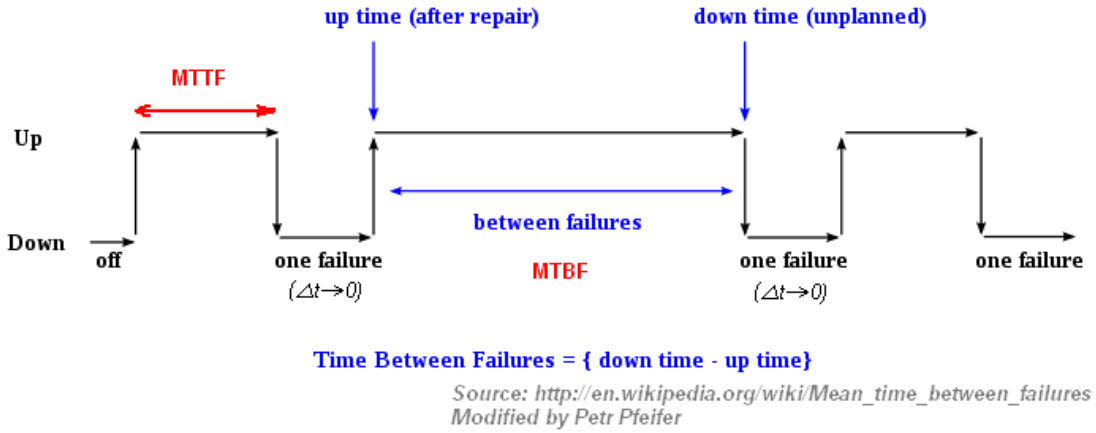

Figure 5. Mean time between failures.

A reliability block diagram (RBD), also known as a dependence diagram (DD), shows how component reliability contributes to the overall aggregated reliability parameters of a complex system. RBD is also known as a dependence diagram (DD). It is drawn as a series of blocks connected in series or parallel configurations, representing each single components of the system with a failure rate. Parallel paths are redundant causing that all paths must fail causing the complete parallel network to fail. Any failure along a series path causes the entire series path to fail.

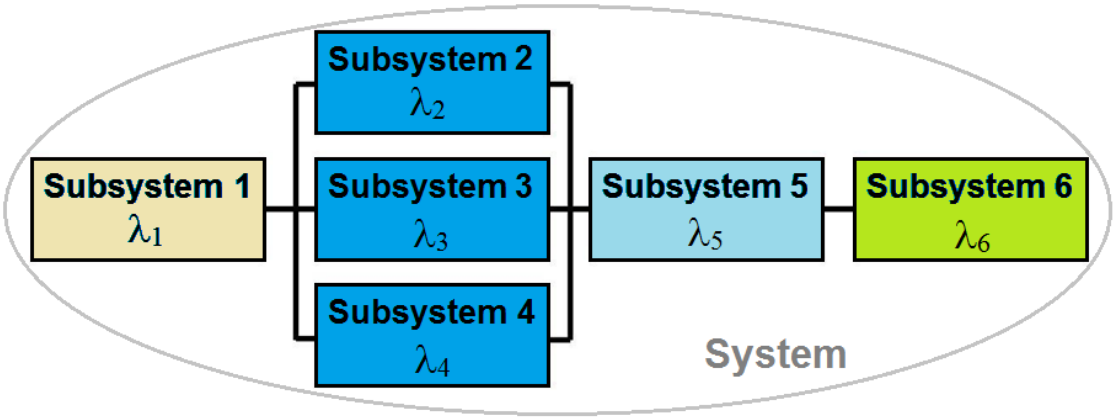

Figure 6. Reliability parameters across the complex systems – a reliability block diagram

2.1 Issues Inherent to CMOS Design

Integrated circuits are made from semiconductor materials such as silicon and insulating materials (silicon dioxide). There are many passive and active components created by various technologies and creating the desired function of the integrated circuit. Complementary metal–oxide–semiconductor (CMOS) is one of the most widely used technologies in integrated circuits. CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions. It has very good noise immunity and low static power consumption.

Figure 7 shows the main issues inherent to CMOS design[1]. There are many other issues related to the testing, packaging and other upper deign level layers, like antenna effects causing corruption of structures during plasma etching process, ESD, etc. Most of such issues can be neglected in case of proper design and manufacturing or storage and assembly phases during the device development, manufacturing and all the device life time. In special cases (equipment with long wire connection in harsh environment), also ESD should be taken into account.

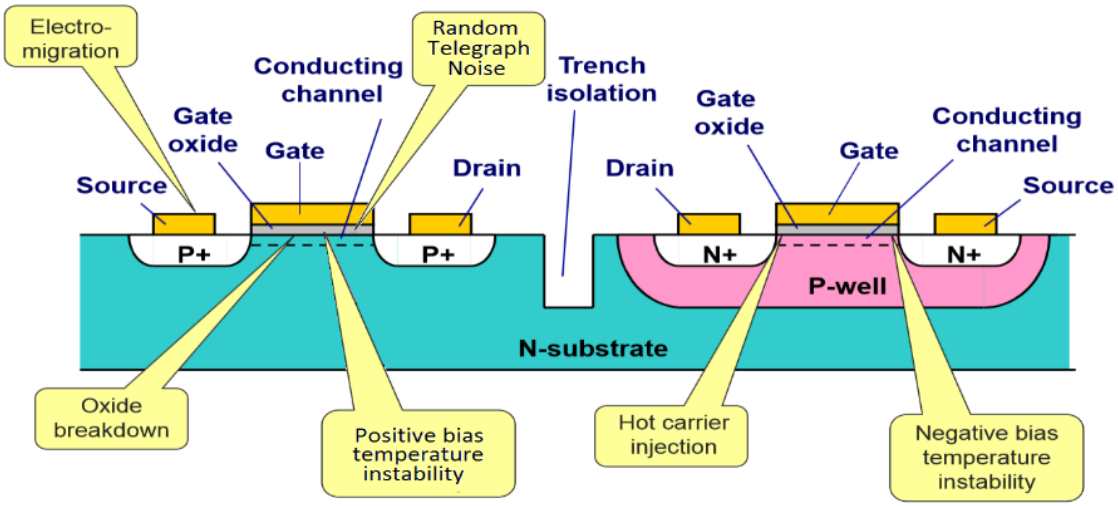

Figure 7. Issues inherent to CMOS design

Most of the strong phenomena cause damage to insulators, weakening of the insulator structures and leading to accelerated breakdown and/or increased leakage, increasing leakage currents in general or in reverse biased state. On the opposite side, a damage to wires and junctions results in increasing resistance, increasing resistance in forward biased state of switches, etc. Increased resistance may result for example in increased rate of electromigration, even above the limit model cases used during the design phases.

BTI and especially NBTI (Negative bias temperature instability) is a key reliability issue in MOSFETs, affecting the gate-channel interface and manifesting itself as an increase in the absolute threshold voltage (even under higher temperature) and consequent decrease in drain current and transconductance of a PMOS field-effect transistor structures. There is nitrogen incorporated into the silicon gate oxide to reduce the gate leakage current density and prevent boron penetration, or alternatives in modern high-*k* metal gate stacks and new materials like hafnium oxides, etc. Also water and many solutions are used during the long and very complex sophisticated manufacturing processes. Obviously, the electric field between the gate and the channel cause creation of interface traps and oxide charge, or migration of sub particles as breaking of SiH bonds at the SiO_2/Si substrate interface by a combination of higher electric

[1] The figure is based on the work of Edward Wyrwas – Physics-of-Failure Approach to Integrated Circuit Reliability, DfR Solutions

field, holes, under temperature, above a certain level of activation energy and over longer time intervals. Hence, NBTI is caused at PMOS transistor structures by long zero/L signal levels at the gate. Therefore the duty cycle (DC) value close to 0 indicates increased probability of NBTI effect at the given signal path. Scaling the technology down, similar effect is also observed in NMOS transistor structures (Positive BTI – PBTI). BTI-inducted delays and timing variations may result in delay faults, propagating up to the device or equipment malfunction or failure, especially in deep-submicrometer devices and nano-scale technologies. The details of how BTI occurs in modern technologies are still not entirely clear, however.

Hot carrier injection (HCI) is a phenomenon where one or more of the charge carriers, an electron or a "hole", gains sufficient kinetic energy in the channel to overcome a potential barrier necessary to break an interface state. The charge carriers can become trapped in the gate dielectric of a PMOS or NMOS transistor and the switching characteristics of the transistor can be permanently changed, causing especially the threshold voltage shift.

Besides the phenomena mentioned above, there are other issues that are typically common to wider set of technologies and structures. For example, time-dependent dielectric breakdown (or sometimes referred as gate oxide breakdown) (TDDB) is a failure mechanism in field-effect transistor structures, when the gate oxide breaks down as a result of long-time application of even relatively low electric field by formation of a conducting path through the gate oxide to substrate due to electron tunnelling current. It is especially when MOSFET structures are operated close to or beyond their specified operating voltages.

In the past years, there were also many issues related to power dissipation (eliminated by proper IC design and packaging), material purity and isotope type or selection issues (emphasizing single-event transition and upset problems especially in 1990's), metastability issues, latch-up (eliminated by actually standard I/O circuits, eliminated on low Vdd technologies and in fact not present on SOI –Silicon-On-Insulator technologies, etc.), antenna effects causing corruption of structures during plasma etching process, etc. seems to be solved for now in very sufficient ways and at many levels. However, the following trends and reliability considerations must be taken into account, reduction of gate oxide thicknesses, reduction of interconnect dimensions, while increasing total wire lengths and number of connections, increasing power densities especially in high-end high-performance devices resulting in thermal issues and higher device operating temperatures, hot-spots, increasing sensitivity to process variations and increase of variations itself, and many new materials introduced or required, while sometimes replacing the old proven ones.

Models for the simultaneous degradation behaviour of multiple failure mechanisms on integrated circuit devices and widely accepted degradation models are available for example from NASA, JPL, University of Maryland, others. Software design tools and large software packs for design of integrated devices and circuits do incorporate them as well. All chip manufacturers do create their own exact models and wide databases, fed by large amount of data available from the production lines, test lines and feedback from the field or customers in general.

The original meaning of the **critical path** was defined as **the longest path**, the path with the longest delay, the longest execution and signal distribution time in a given design or its subset or circuit. Such a path typically determines the maximal working frequency of the given synchronous system - the maximum possible clock rate in the system is determined by the slowest logic path and the parameters of the clock distribution network. Introducing the matters of the wide range of negative and degradation processes, the critical path raised the need of a new term or a redefinition this original one in the way, that it has to be the path, which **can potentially stay the longest one**(s) **within a given time frame,** and/or **under given conditions**. It also is called the **aging-critical path**, especially in the case, when this path degrades in some important parameter(s) in the fastest way.

3 Description of the New Method

The ASIC test ring oscillators are typically designed as a series of transistors or any basic structures in such a way which allows oscillations in the chain and generation of desired signals. The test rings consist of *n* stages or repeated structures. It has to be noted here that the presented method is primarily based on only 1 inverter (logic gate) plus *n-1* delay stages. In other my experiments, where *n* inverters were utilized in the ring chain, the rings were too sensitive to the power conditions and generated too high noise. It is one of the biggest differences to most of designs and methods that are used or can be found in industrial or research papers.

The method utilizes BRAM (Block RAM) and undersampling within corresponding Nyquist zones, delivering relative as well as absolute data. Duty cycle can be also calculated very easily. The presented method allows both the external as well as complete in-situ data acquisition and processing. Me and my colleagues have already presented a VARP VLIW solution in [*66*] and [*67*], allowing complete, extremely easy and low-cost implementation of the method into soft-cores on many Xilinx and Altera platforms. In addition, this solution can be directly combined with the novel XOR-less aging detection unit, introduced in [*44*]. The data can be processed directly on the FPGA chip or by an external PC (offline). The original usage of the developed solution was for the purposes of aging measurement; however the method has much wider usage.

When incorporated in some final design, the selected (measured) or critical path aging effects can be estimated based on the measurement of duty cycle of the signal. As reported many times, NBTI (Negative bias temperature instability) is caused at PMOS transistor structures by long zero/L signal levels at the gate; hence duty cycle DC in value close to 0 indicates increased probability of NBTI effect at the given channel. Scaling the technology down, similar effect is observed also in NMOS transistor structures (Positive BTI – PBTI).

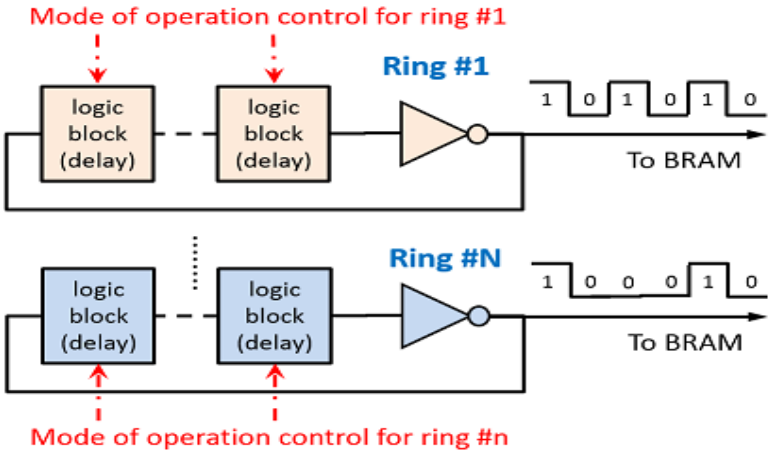

Figure 8. The first part of the basic principle of on-chip parameter measurements.[1]

The results of measurement of the SLICE or CLB parameters presented further in this document were obtained by a frequency measurement method, delivering very stable results and capable of measurement of delays with the resolution in the range of 0.1 ps (typically 100 fs, in some cases the resolution can be better, but it could be influenced by the noise level among the circuit modes). It is possible to perform the measurement without a need of any external equipment, utilizing just one precise on-board 100MHz or 200 MHz crystal or MEMS-based oscillator as the base clock frequency used in most of high-end solutions today. This value of the reference frequency was selected because of its simplicity and also it is selectable all across the main development kits and platform.

The method typically allows measurement of parameters of the FPGA basic configurable units, however also measurement of internal circuits and devices down to CMOS inverter or

pass-gate levels is possible even within selected, already existing and available types of programmable integrated circuits. Special modes of operation allow reconfigurations in the number of active stages or set up the active stress voltage levels all along selected temporarily inactive ring oscillators. A *differential* method (e.g. BTI impact and reliability assessment purposes, [*68*] or [*69*]) compares on-line a path of selected ring in stressed mode 0 or 1 to another ring, typically oscillating all the time. The result sampled to memory is directly the difference between selected 2 ring oscillators. It is suppressing supply voltage and the die temperature variations much better, than in the case when the rings are compared fully separately. Advanced delay-fault detection mode [*44*] can be used. Data from dedicated units like in [*64*] can be internally utilized as well.

Advanced 40 nm technology as well as the newest successful and widely used 28 nm technology is very fast, therefore most of the test ring oscillators were designed as addressable four-stage rings. See Figure 9 and Figure 10 with the example of the exact implementation of the rings in Xilinx FPGA. Only 35 selected rings were designed as much longer, allowing generation of frequencies below the sampling frequency *fs*. The extended version of the solution uses programmable number of stages in each ring, however the set of possible lengths of the ring and number of the CLBs in the chain must be specified during the design phase. **Each stage utilizes one LUT** and one flip-flop in the **latch** mode (single SLICE). Only **the last stage** in each ring **inverts** its input in order to create the ring oscillator. Each ring has one **enable signal** and one **special signal**, determining level 0 or 1 across the whole path **when the ring is disabled** (off). The last signal allows a change in the ring structure and can control the total length of the chain. The output of the ring and dedicated BRAM bit or data stream will be also named a "channel" in this document.

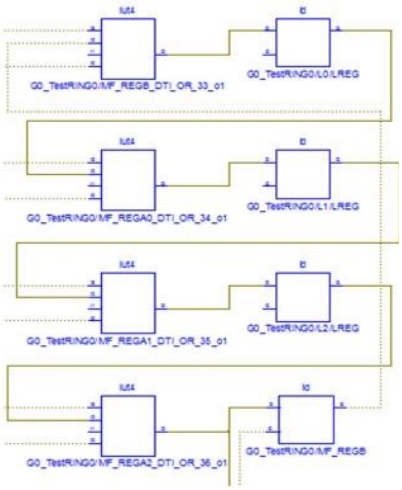

Figure 9. An example of the implemented short ring.

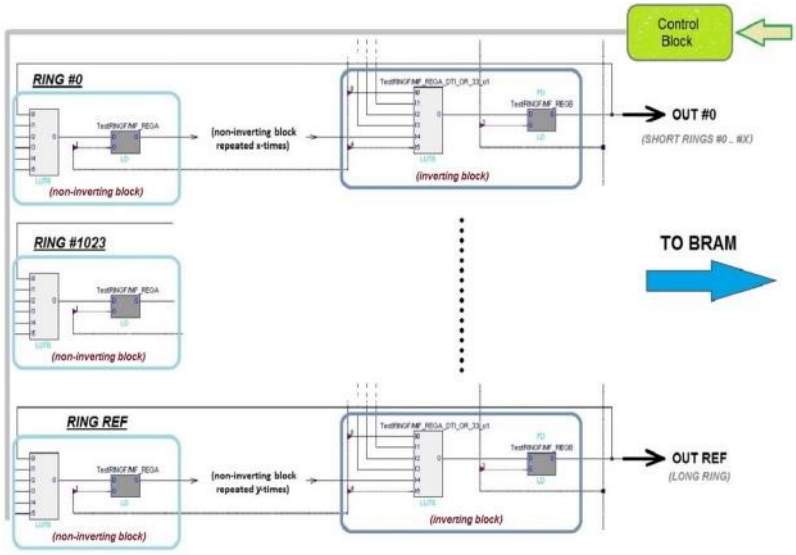

Figure 10. Implementation of test rings and control signals.

The last version of the test rings has also introduced a programmable length of the rings, where the new signal can change the length of the ring, allowing oscillations generated by various number of the basic logic units while maintaining same location of the measured test structures without special constraints. It enables a completely new dimension of the measurement itself as well as advanced data processing using different data and calculations on same structures, however running in different modes of operations or influencing each other in different ways.

The ring oscillators and their parameters or control signals can be programmed by a separate control chain(s) in most of cases and especially in non-reconfigurable types of FPGA

or programmable devices, like Altera or Lattice FPGAs or CPLD (Complex Programmable Logic) devices using e.g. Flash cells or hybrid structures. In reconfigurable types of programmable devices (Xilinx FPGAs), all the ring oscillators and their parameters or control signals can be programmed or read back to the main unit by a special configuration streams. If properly solved at the synthesis levels, the final design will contain more oscillators to be used for the measuring purposes and also the spectrum of the measured parameters can be wider or the overall granularity can be finer.

The whole design, written in Verilog (description in [*70*]) , incorporates an array of up to 1024 addressable two-stage ring oscillators in total, each of them can be separately switched on (enabled) and off (disabled) by its dedicated enable signal. In addition, the off-state can be also fully controlled, as mentioned in the previous subchapter. This feature is used for the **study of aging effects** and change in parameters of PMOS (marked as zero/0/L) or NMOS (marked as one/1/H) state applied for long time to selected set of rings, while others (marked as X) can run for days, weeks or months. In addition, the complexity of the solution results in different final design of each single ring – some are designed utilizing local routings, some as near-by SLICEs or CLBs. In the final set of 1024 rings, subsets of selected rings were identified, based on timing or location constraints or interests, some with near same parameters, each belonging to selected group of always-running rings, or rings with temporary 0/L or 1/H state.

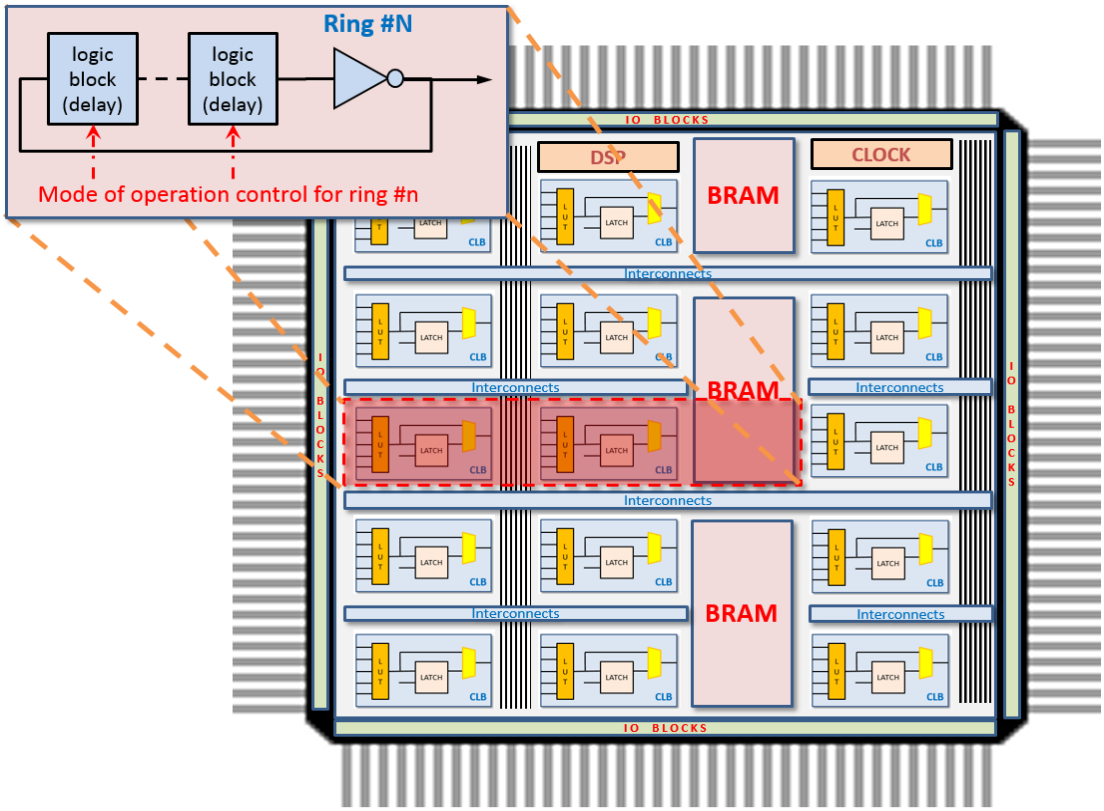

Figure 11. A general implementation in programmable technologies and the general principle in an illustrative way.

The presented approach is new in its background as well as application. However, and in addition to such approach, the overall method simplicity and quality of the results is increased by utilization of Block RAM units (BRAM) in modern FPGA devices. It enables a new dimension of measurements and data acquisition. The Block RAM units implemented in modern devices incorporate true dual-port 8-transistor cells in RAM blocks. In addition, such

blocks incorporate perfectly synchronized samplers as a series of D-type flip-flops (DFFs) integrated at all the data and address bit inputs, control signals and optionally at the data outputs (such output flip-flops can be bypassed, while the input ones are fixed in the BRAM functional block).

A very typical block RAM logic diagram used in near all modern FPGA devices consists of a memory array, latches and input and optional output registers. This basic (single data bit) unit is implemented in 18 or 36 copies utilizing the same address, clock and mode or enable inputs, while sharing area in the same dedicated locations across the FPGA die. In some types of FPGA, the memory blocks can also be routed in a cascade mode creating a large dual-port 36 Kb block RAM with port widths of up to 72 bits. The length of memory block is configurable with respect to the number of used data bits. The extended size of data bits allows optional error check and correct (ECC) function by implementation of parity or similar memory data content checking and also correction mechanism. The memory block provides one additional data bit per each group of standard 8 data bits. The input data and registers are sampled in all modes of operations, the output register can be used or passed by the output multiplexer. Each memory access, read or write, is controlled by the clock, all inputs, data, address, clock enables, and write enables are registered. Nothing happens without a clock. During a write operation, the data output can reflect either the previously stored data, the newly written data, or can remain unchanged. A programmable FIFO logic is implemented in some FPGA families as well.

The memory blocks are populated in high numbers all across the FPGA die. It is obvious that the number of BRAM blocks is much lower than the number of other logic components. The entire pool of configurable logic blocks (CLBs and SLICEs) is interleaved by BRAM blocks or dedicated DSP (digital signal processing, multiply and accumulate) blocks. BRAM modes The Block RAMs circuits can be configured in various modes, these modes represent the final data and address configurations and may limit the size of the basic block or a chunk of data in the final data stream. FPGAs manufactured using 28 nm technology (TSMC) have some new features, like power gating implementation (unused blocks are completely switched off) and also the new external power supply V_{CCBRAM} is used to power the block RAM memory cells.

Table 1. Number of available BRAM blocks present in various Xilinx FPGA families.

Family	*Technology*	*BRAM blocks (min.)*	*BRAM blocks (max.)*	*BRAM Size Total (max.)*	*Source*
Virtex 5	65 nm	36	516	18,6Mb	[*75*] DS174 (v2.0), [*76*] DS192 (v1.3)
Spartan 6	45 nm	12	268	4,8Mb	[*77*] DS160 (v2.0)
Virtex 6	40 nm	156	1064	38Mb	[*78*] DS150 (v2.4)
Artix	28 nm	50	365	13Mb	[*79*] DS180 (v1.15)
Kintex	28 nm	135	955	34Mb	[*79*] DS180 (v1.15)
Kintex Ultrascale	20 nm	540	2160	76Mb	[*80*] DS890 (v1.3), [*81*] UltraScale Architecture Product Selection Guide
Virtex 7	28 nm	795	1880	68Mb	[*79*] DS180 (v1.15)
Virtex Ultrascale	20 nm	1260	3780	136Mb	[*80*] DS890 (v1.3), [*81*] UltraScale Architecture Product Selection Guide

Regarding the required number of memory blocks, the number of BRAM blocks in FPGAs is typically not aligned to 2^n (it means 256, 1024, 4096 blocks) and thank to this reality and typical size of cache memories, some BRAMs stay unused in most of designs. Table 1 shows numbers and total sizes of BRAM blocks available in each modern product line and FPGA families. My measurement blocks and delay-fault detectors can use just such spare blocks. In addition, they can use only interconnect resources or minimal spare logic resources. In most of cases, my aging detectors do not affect the original design the FPGA designs updated of the aging and reliability measurement units.

Figure 12. Size of BRAM blocks available in various modern Xilinx FPGA families.

Figure 11 shows an overview of Table 1 in graphical illustrative format and shows also the trend, clearly indicating strongly rising the total number and capacity of BRAM blocks in modern FPGAs.

Figure 13 illustrates the key part of the method and the usage of BRAMs, where waveforms of ad-hoc created oscillators are streamed and sampled into memory blocks of size n bits. As the main key outputs, duty cycle (shortened as DC) and frequency are calculated, resp. the relative zone frequency (shortened as CH) in active Nyquist zone k of the sampling frequency f_s. The relative zone frequency of all the circuit or delay t_d per one stage of s-stage long ring oscillator can be calculated for given data stream using simple linear formula, very effectively implementable in software or hardware resources.

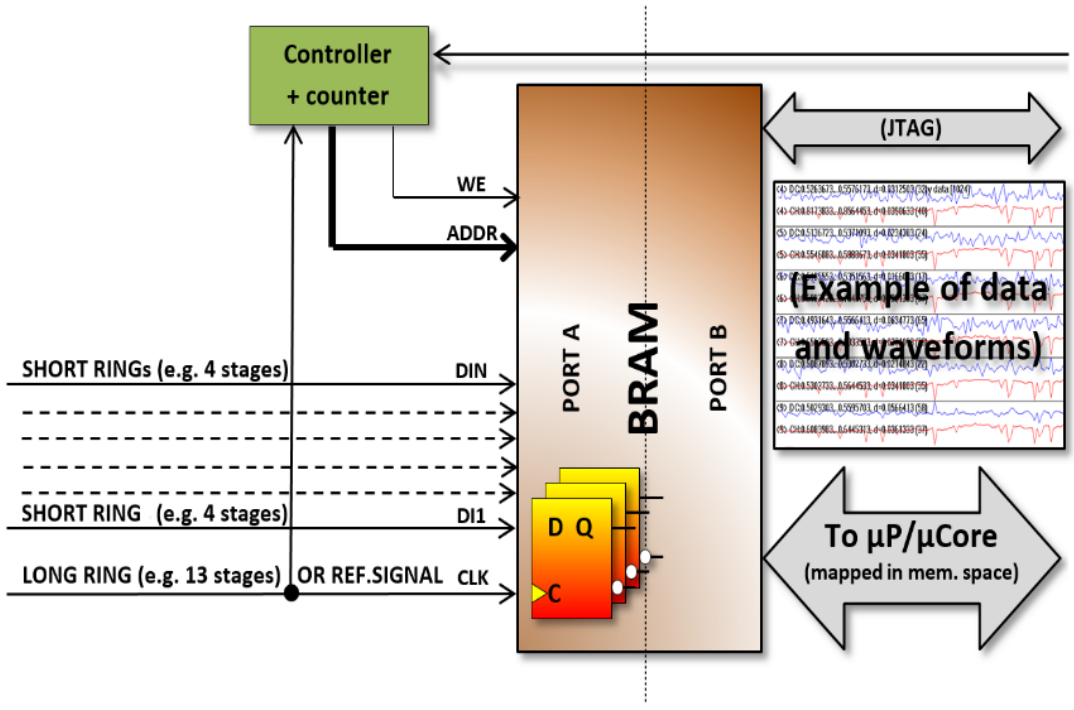

Figure 13. The basic principle of the method and complete on-chip parameter measurements using BRAM blocks.[2]

[2] Multiple digital oscillators across the chip and the resulting data streams are sampled in the synchronous memory block. The entire area and circuits of chip can be measured and processed using e.g. partial or dynamic reconfiguration.

The method can also be implemented using sets of counters. However, simple design, implementation, extensibility and wide are new and unique advantages of this new method. The design and implementation remain same for all the evaluation processes as well as source of data. In addition, this method allows processing of partial data streams utilizing the same resources. For example, ring oscillator start-up phases as well as steady oscillation phases can be analysed in the same BRAMs and data streams by changing the start and stop addresses. No any special set of programmable counters and logic is required at all – only one tiny and easily implementable fixed set of already presented dedicated resources is connected to already existing designs using interconnect resources only. In addition, such BRAM blocks can be still utilized as a standard RAM memory in processor systems, if the measurement tasks are not in process. Memory segmentation techniques are available as well.

3.1 Nyquist zones and undersampling

When the ring outputs are latched, acquiring bits or data from the ring oscillators and channels and creating the data streams, sampling is performed as the key process of converting a signal into a numeric sequence. The Nyquist–Shannon sampling theorem, named after Harry Nyquist and Claude Shannon, more commonly referred to as the Nyquist sampling theorem or the sampling theorem, is the fundamental result in the field of information theory, and it says that if a function *x(t)* contains no frequencies higher than f_n hertz, it is completely determined by and can be reconstructed giving its ordinates at a series of points equidistantly spaced $1/(2 f_n)$ apart, or a given band-limited function can be perfectly reconstructed from a countable sequence of samples if the band limit $f_s/2$, which is no greater than half the sampling rate *fs* (in Hertz or Samples per second). The half-period from DC (zero frequency) to $f_s/2$ (half the sampling frequency) is often called the *Nyquist interval* or the *Nyquist region* or the first *Nyquist zone 0*. The $f_s/2$ is called *Nyquist frequency*. The band from the Nyquist frequency fs/2 to the sampling frequency *fs is* the *Nyquist zone 1*, and so forth. This key theory is all well-described and referenced in all literature and sources dealing with sampling or signal processing methods or technologies, starting from the key famous paper [*82*], followed by a comprehensive overview presented in [*83*].

Figure 14 describes it in detail and shows an example of the signal spectrum, Nyquist zones and undersampling.

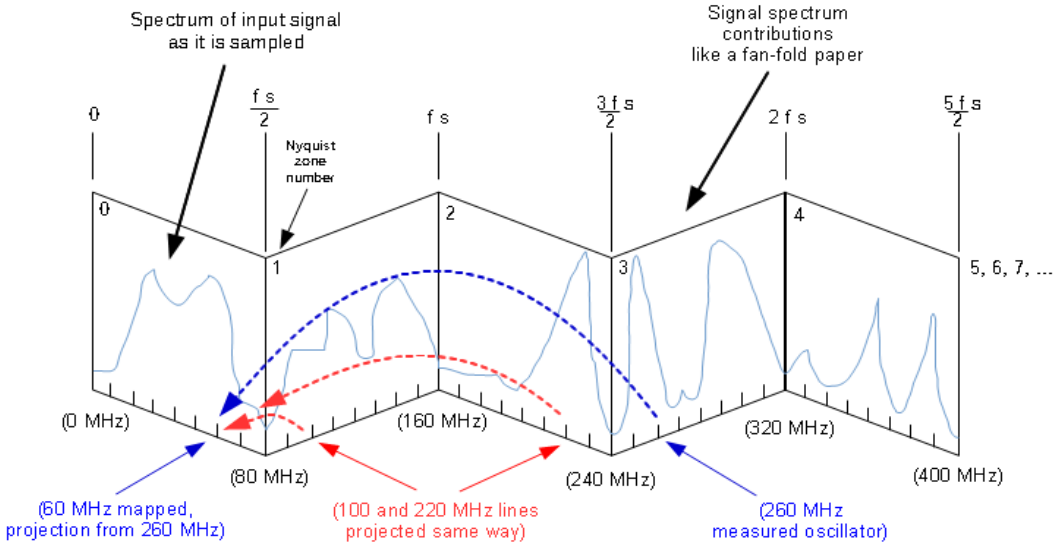

Figure 14. Signal spectrum and an example of undersampled signals

Undersampling or bandpass sampling, in general, is a technique where the signal is sampled at a sample rate below its Nyquist rate or twice the upper cut-off frequency, but one is still able to reconstruct the signal. It means that a given signal can be sampled by another, much lower frequency signal, while same parameters of the given signal can be still reconstructed. However, when one undersamples a bandpass signal, the samples are indistinguishable from the samples of a low-frequency alias of the high-frequency signals. Hence, e.g. the frequency of the given signal f_g sampled at the rate of f_s cannot be determined without previous knowledge of the exact number of its Nyquist zone, because the data sampled and results calculated are de facto invariant to the number of the Nyquist zone, as the general theory shows.

Any purely sine-wave unit signal results in a single solution and just one Fourier coefficient. Periodic functions defined on the unit circle are simply projected by the Fourier transform to the sequence of its Fourier coefficients. A harmonic of a wave is a component frequency of the signal that is an integer multiple of the fundamental frequency. When this fact is simplified to the presented undersampling approach, the Fourier analysis shows that only periodic signals with duty cycle 50% sampled by and ideal signal and equidistant sample points may result in a single unique result. A signal with its duty cycle not equal to 50% (the duration of zero or one in purely digital binary representation) must result in multiple frequencies in term of its absolute fundamental as well as all the spectrum of their harmonic components. Therefore, the frequency of such signals cannot be explicitly determined by the undersampling method and such values of the duty cycle will result in an error in measurement or even complete impossibility to calculate or determine even basic components of the sampled or signal measured. The following lines show it all in a very illustrative way.

3.2 Evaluating duty cycle

A duty cycle (or duty factor) is typically defined as percentage of time that an entity spends in an active state as a fraction of the total time under consideration. A standard formula can be used to calculate the Duty Cycle (DC) of the selected signals as follows:

$$Duty\ Cycle = \frac{\tau}{T} \tag{3-1}$$

where

τ is the duration of 1 (is active state H or logic 1),

T is the period.

Using a probabilistic approach and sampling the signal at random uniformly distributed time points as well as sampling the data signals asynchronously - it means the sampling signal is different from its component in the Nyquist interval in its frequency, allowing to sweep the sampling point along the basic signal interval - we get:

$$Duty\ Cycle = \lim_{n\to\infty} \frac{\sum_{j=1}^{n} x_j}{n} \approx \frac{\sum_{j=1}^{n} x_j}{n}; \forall n \gg 1 \tag{3-2}$$

or

$$DC = \frac{\sum_{j=1}^{n} x_j}{n} \tag{3-3}$$

where

n is the number of samples in BRAM,

x_j is the j-sample (sampled 0 or 1),

and DC is in the range of <0,1>.

As mentioned above in the theory subchapter, the duty cycle information is important information in determining the frequency of a signal. However, changes in the duty cycle may be efficiently used in an analysis of the signal path and determining for example NMOS or PMOS field-effect transistor gate threshold values. In an ideal case, if the threshold is set at a half of the circuit power supply voltage, and the delays in the circuit are the same for both L to H and H to L (the circuit and entire path has sufficient bandwidth and it transports a signal transition in exactly the same way), the duty cycle of such a signal sampled by an ideal sampler with zero jitter and the same threshold value will result in the same number of zeroes and ones in a sufficiently high even number of samples in sampled data streams. The even number of samples is already ensured by the length of the memory blocks, typically 2^{bn}, where bn is typically 10 in modern FPGA devices, enabling typically 1024 memory rows and 18 or 36 data streams per each single BRAM unit.

3.3 Evaluating frequency

If sampling periodic signals with a duty cycle very close to 50 % (H:L levels of the digital signal in their length close to 1:1), the following evaluated formula for undersampling and the corresponding Nyquist zone can be used and the frequency calculated easily from the data, using a linear or hyperbolic format and corresponding algorithm. However, precise measurement of the frequency in terms of its absolute value is not required at all. In fact, the only parameter measured is the change of frequency within a Nyquist zone. Therefore, in the following linear formula, only the value of CH is to be evaluated as a relative number of transitions in the sampled data streams, such as:

$$CH = \frac{\sum_{j=2}^{n} |x_j - x_{j-1}|}{n} \tag{3-4}$$

where

n is number of samples.

x_j is the j-sample (sampled 0 or 1),

and CH is in the range of <0,1).

In this case, the subtraction and the absolute value can be calculated using the XOR (eXclusive-OR, symbol ⊕) logic operation. This logic operation, as a logic gate, is already present in high amount in the configuration logic blocks in programmable logic devices, including FPGAs and CPLDs. Using this XOR-gate already present in the chips, **no** any special or any intensive logic resources are required at all. It also is one of the very basic operations supported by all ALU (Arithmetic Logic Unit) in processor systems.

Using the XOR operation, we get the following formula:

$$CH = \frac{\sum_{j=2}^{n}(x_j \oplus x_{j-1})}{n} \tag{3-5}$$

If *DC* is 50%, the frequency (linear formula) can be calculated as follows:

$$f = \frac{f_s}{2}(k+m) - \frac{f_s}{2}\left(sgn(\mathrm{m}-1)\right)\left(\frac{\sum_{j=2}^{n}|x_j - x_{j-1}|}{n}\right) = \tag{3-6}$$

$$= \frac{f_s}{2}\left(k + m - sgn(m-1).\left(\frac{\sum_{j=2}^{n}|x_j - x_{j-1}|}{n}\right)\right); n \gg 1 \tag{3-7}$$

Hence, the average delay of each single stage can be calculated as:

$$t_d = \frac{1}{S.f_s.\left(k+m-sgn(m-1).\left(\frac{\sum_{j=2}^{n}|x_j - x_{j-1}|}{n}\right)\right)}; n \gg 1 \tag{3-8}$$

where

fs is the sampling frequency,
k is the active Nyquist zone number (0,1,2,3, …), while the first Nyquist zone (here starting from number zero) is 0 Hz to *fs/2*,
m is *k* modulo 2,
S is the number of stages in the ring oscillator.

As mentioned in the theory subchapter above, in order to exactly determine or calculate the frequency of the digital signal, its duty cycle must be equal to 50 % and also the sampler (sampling unit) has to have ideal parameters. Figure 15 shows the impact of the duty cycle ratio on determining the frequency as it was introduced above.

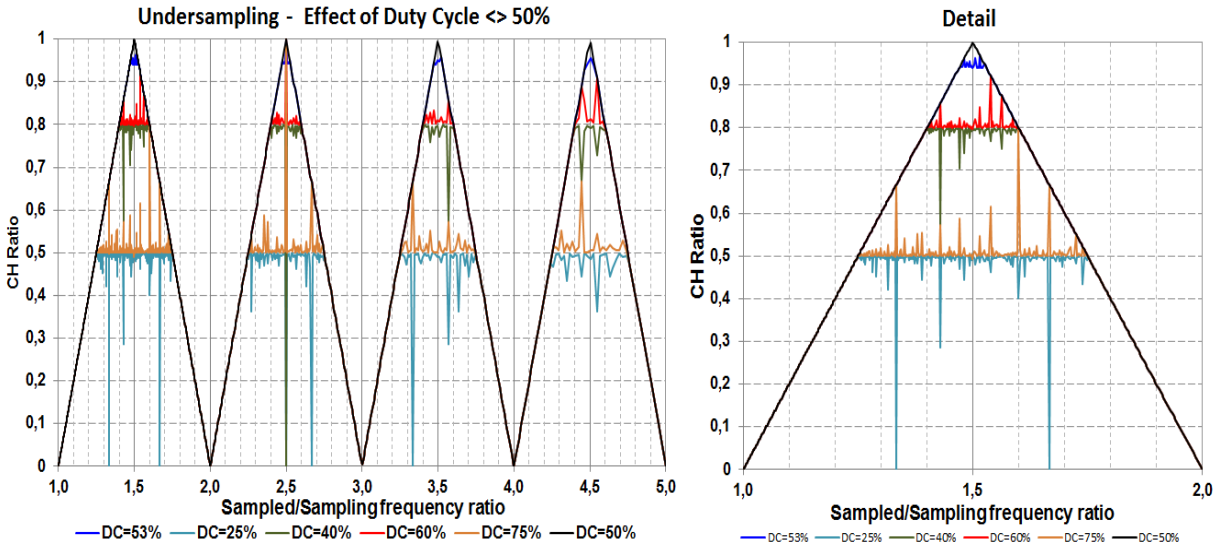

Figure 15. Simulated effect of duty cycle on frequency evaluation (with detail).

Not only the theory, but also the simulations performed as well as real tests show, that duty cycle DC of 50±3 % as well as the typical jitter in the range of picoseconds causes acceptable error below 10 %, while the results can be finally adjusted under certain conditions. In case of changes in DC while CH stays the same, it is obvious, that we are facing some change of the circuit or FET transistor threshold levels. Any changes in the frequency are caused by variations in voltage of internal power supply rails or die temperature.

3.4 Absolute and differential method

The new proposed methodology allows implementation of two key methods, called *absolute* and *differential*. The absolute method uses an external signal as the clock signal of the sampler unit or the BRAM clock input. It utilizes typically 100 MHz clock signal as the source of sampling frequency from the on-board crystal oscillator unit already present on most of development boards and kits. If the stability and quality of the oscillator and all the signal path is high, the method is surprisingly sensitive to detect very tiny changes in temperature or power supply voltages, and the resolution is sufficient enough to detect a human finger is touching the FPGA package (the sensitivity is approximately 0.7 ps/K in case of 45 nm low-power Samsung technology [*84*]) as well as stress effects in the FPGA silicon substrate due to e.g. torque, moment of force applied to the FPGA package or the whole PCB board. Random telegraph noise (RTN) exhibited by deep-submicrometer metal-oxide-semiconductor metal–oxide–semiconductor field-effect transistors can be detected as well. **The absolute method is used mainly for measurement of parameters of the basic units of the devices, delays, strong crosstalk, mutual changes in threshold values and dependencies of the internal structures to e.g. temperature or voltage absolute values or variations.**

The new differential method is a completely new method invented. In this case, the clock source of the sampling unit or the BRAM clock input is connected to another selected ring oscillator output, typically much longer in its number of chain units, or in having specific parameters. This solution creates **completely in-situ method**, because the measured objects, the measuring unit, data acquisition and data storage unit as well as the data processing units are on the same chip, device or in the same package. Owing to this fact, all the parts of the solution do have same or very similar environmental conditions, while utilizing different sets of transistors or basic circuits, paths and logic blocks. This solution suppresses the effects of temperature changes to acceptable minimum levels (an increase in temperature by 40 degree of Kelvin represents typically only about 10 % of measured aging effects per month) even on its very basic data processing level. **The differential method is used especially for aging and device degradation processes measurement and analysis purposes. If combining advanced matrix operations and data from measurements using also the absolute method, electromigration effects, various crosstalks and other mutual effects as well as tiny changes in the device can be detected at much higher sensitivity levels**.

3.5 Method's sensitivity and resolution aspects

In the case of the absolute method, the overall quality of the outputs generated by the method presented is determined by the external clock sources and quality of the signal paths to the device. In both cases, both mentioned key parameters of the method are directly affected by the amount of data available in the data streams. However, the maximum BRAM sampling frequency is limited to those around 300 MHz in low-power or 600 MHz in high-performance modern FPGA devices. Also the jitter caused by the BRAM input units, crosstalk,

interconnections, and consequently data samples, creates additional errors in the measurement. Figure 16 shows the results of experiment, where the sampler shows uniformly distributed jitter at various levels. The results clearly show that the error caused in measurement of the signal frequency is below 2 % in the first Nyquist zone and the number of stages used in the ring oscillators. It is highly limited close to the limits of the frequency band, while the measurements at the centre frequency are nearly unaffected.

The length of a data block obtained per one cycle is in MB (4Kb to 64Kb per channel). In case of higher number of rings, each data path consists of 1024 bits. During the tests, the length of data in 1 kbit per channel was observed as the minimum to get some reasonable outputs. Arrays larger than 64 Kb provide no significant improvement in final results. The raw data can be extremely easily compressed by a simple lossless compression method (for example run-length), or advanced compression method like Huffman compression, LZW, etc.). The data can be processed by the internal processor (typically ARM processor cores on modern FPGA devices, or any type of soft-core processor solutions, such as Microblaze in my case) or sent out of the chip via USB or JTAG to a PC and processed there. The way of utilization of BRAM and the presented algorithms are suitable for multicore systems and multiprocessing as well.

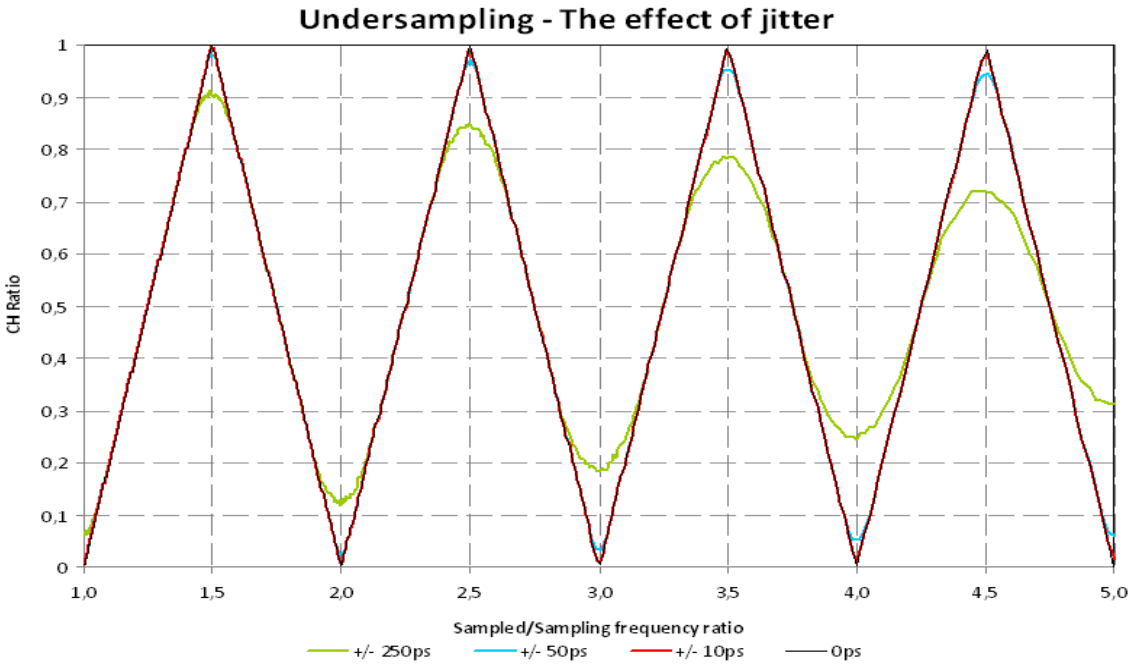

Figure 16. Simulated impact of jitter of sampler on frequency evaluation.

For the absolute measurement mode, just one precise on-board crystal oscillator is utilized as the base clock frequency, typically 100 MHz or 200 MHz. This value was selected because of its simplicity and also because it is selectable all across the main development kits and platform. Theoretical resolution of the method is limited by the maximum sampling frequency and length of the sampled data block. Theoretical resolution of the method is obviously limited by detection of at least one difference in two data streams of two sampled frequency sources or outputs of ring oscillators.

The real usable and stable values of the method's resolution, on real structures and using full BRAM data width, are typically in the range of tens of picoseconds, also due to jitters, wider aperture window and lower BRAM clock frequencies used in most of designs.

3.6 Delay-Fault Run-Time XOR-less Aging Detection Unit Using BRAM in modern FPGAs

The reliability issue, including aging processes in modern devices with very fine structures and utilizing programmable technologies, being applied in high-performance or dependable systems in various safety, automotive or space applications, is sometimes very difficult to predict, measure or watch. The task is well-mastered in the world of ASIC, the situation is slightly different for FPGA devices. Modern FPGA devices incorporate number of true dual-port memory blocks with 8-T cells, hence offering new options. However, such blocks are typically used for data storage and processing purposes. This chapter presents my completely new solution as a new way of utilization of the RAM block (BRAM) for the delay fault detection purposes. The BRAM and a simple controller log risky transitions or delay fault events and may positively affect the overall reliability of the device as well as all the system.

The aging of the electronic nanostructures, as well as the most of the generally negative internal changes due to various physical mechanisms, causes changes in parameters of CMOS structures; PMOS transistors are more sensitive than NMOS. It typically results in changes in the gate threshold levels or interconnects (electro-migration). These changes also result in lowering of the maximal drain current and cut-off frequency, elongating the processing delays in the aging-affected circuits (compared to the original design). An overview of the aging issue and solutions in FPGA can be found e.g. in [*124*], the degradation analysis can be found in [*14*], interconnects delay issue is described in [*125*]. In case of dependable systems, the key parameter lies in the negative changes in delays of critical paths. The system failures due to such negative effects must be avoided. Hence, all the critical changes have to be detected, in the ideal case the given or sufficient time before it results in the system failure.

One of the possible solutions is to measure changes in internal structures, typically propagation delays of selected signals with automatic detection of events above given limits. As long as the timing requirements of all paths are correct, lowering maximal working frequency of transistors or structures doesn't affect the overall reliability of the circuit or system. Aging stays visible and causes problem only if the propagation delays in implemented logic path exceed the given values. The usually used technique of detection of the timing violations is to generate another auxiliary clock signal and sample the end of the critical logic path twice with a short mutual delay. It means to sample the output of latches or D-Flip Flops (DFF) of selected paths at two (or more) time points around the original (global) clock rising (or falling) edge, and compare all the output values, typically by XOR gates. In critical paths and during work of dependable systems along their lifetime, no any change of the output of the logic part of the design (routed to the DFFs input) is permitted within the given setup and hold timing constraints [*85*] and [*86*]. When the output values differ, one (or more) of the first in line latches or other DFF has probably sampled a wrong value. It means that a metastability or SET/SEU (Single-Event Transition/ Upset) has occurred. If signals with those wrong parameters are propagated in the system or processed by following circuits, it may cause wrong functionality of the circuits or device. It directly influences the internal functionality and reliability of the dependable system.

It is very difficult to find papers or previous work about aging detectors using BRAMs, as well as other results from this area in FPGAs. However, the work described in [*126*] shows sufficient stability of the internal FPGA structures, including the front DFFs of the BRAM blocks (see [*72*] or [*71*] for all details). As mentioned, the BRAMs are typically used for data storage or processing purposes. However, the BRAMs in modern FPGAs offer many new options, they have been improved (see [*72*], [*71*], and [*127*], and their reliability is similar to

the rest of the chip area of devices nowadays, for example [*43*]). In addition, high-quality externally-inducted-SEU-free devices (Actel, BAE, and other military grade devices) already exist, while one of the biggest issue – aging effects – remains and gains with lowering of lithography technologies.

Figure 17 shows the basic idea of the new solution. It is obvious, that it is only an extension of the standard solution, while the delay-fault detection DFF is replaced by the BRAM resources, already containing very well synchronized DFFs in the front stage unit (described in [*71*], [*72*], [*85*] and [*86*]). Moreover, this my solution doesn't incorporate any XOR gate to be added to the original design. During the implementation of the presented solution, it was found that the interconnect network delays (NET), in the CLBs and crossbar switch arrays, are in the desired time range. The clock distribution network and paths are quite well designed. And in some cases, only the delays of interconnect paths can be utilized. The final solution should avoid a must of processing of data stored at different rows (memory address or sampling time). The already latched signal (output of the BRAM) is routed back to the BRAM and latched again in the next cycle. It ensures the desired time independence of rows in the memory. It is obvious, that this approach and way of implementation in fact completely isolates all the events. Each memory address location (row) and data in the BRAM can be processed as fully separated events. The XOR operation is performed by the CPU operation. However, the memory locations can be written and read fully asynchronously, while no any extra read cycle or existence of the previous corresponding data is required.

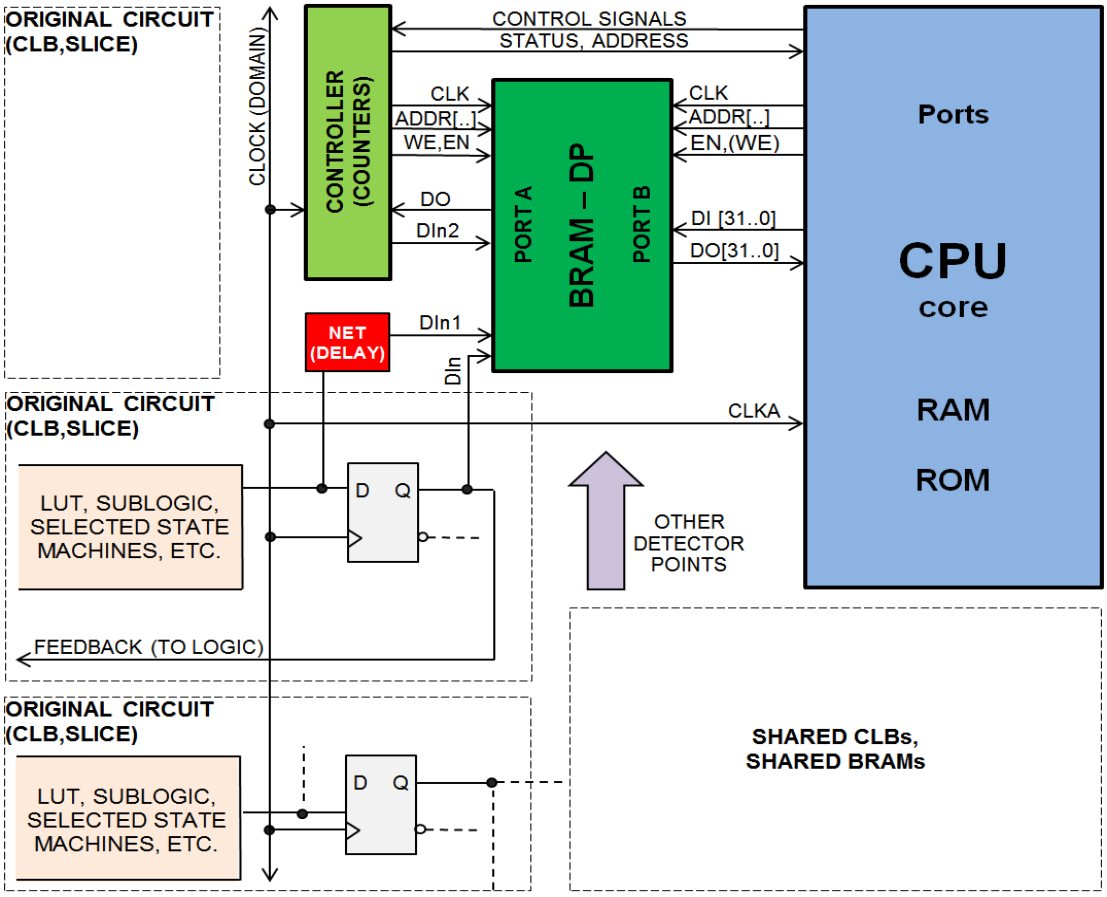

Figure 17. Main idea of the new solution (no XOR gate is required)

The detailed timing parameters of the final design can be obtained from the design analyses, or results from PlanAhead (or any other tool), or it can be measured as well. For the direct measurement purposes, it is required to implement only one diagnostic signal, in the best case

allowing generation of periodical signals in the critical path. Some systems already incorporate such feature for self-checking purposes; thus no any other signals are required. The signal must be generated fully asynchronously to the clock signal, or synchronously with well-defined L and H widths, jitter or time delays, allowing calculation of the aging detector unit parameters. The tests performed with fully asynchronous signals clearly showed, that the results are surprisingly very stable, and in the required range of tens or hundreds of picoseconds.

Figure 18 shows the simplest implementation of the solution. It presents only the main idea. The virtual zero delays are never present in any real system. The simplest solution gains just from the existence of significant interconnect delays. The delays must be determined or designed in order to setup required delay sensitivity. This complex solution can be insufficient in some systems, but many systems can utilize just this simplest solution. It was previously validated on the test systems (with Xilinx Spartan 6 and Virtex 6 FPGAs), that the interconnect delays can be quite short in the range of hundreds of picoseconds (with subsets in tens of picoseconds), depending on the type and length of interconnect. These delays are fully sufficient to cover setup/hold times.

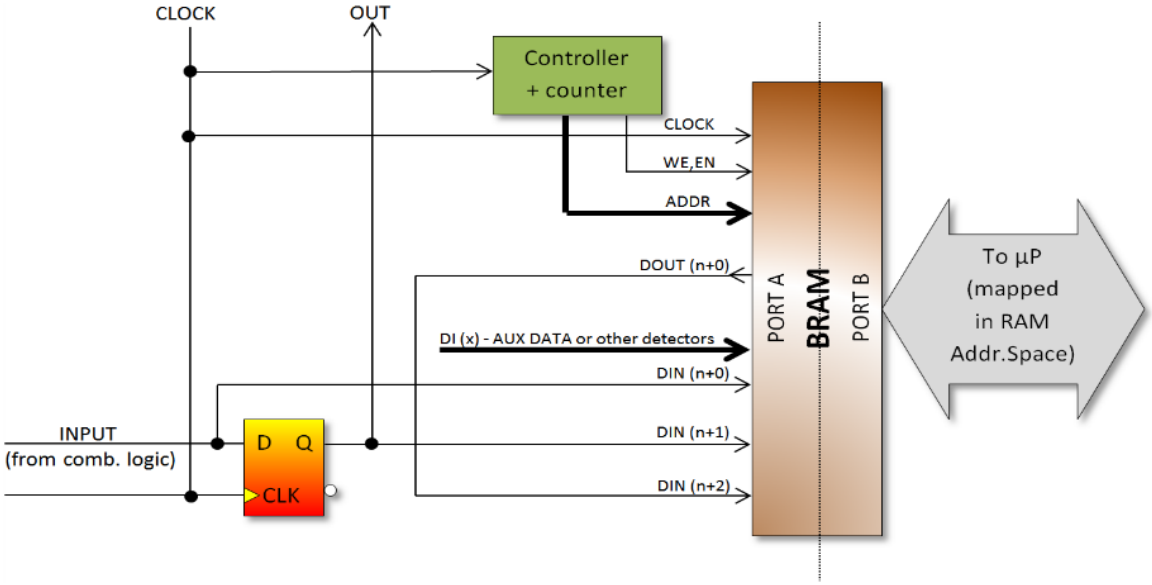

Figure 18. The very minimal version of the proposed detector – no any SLICE or CLB resources are used for XORs

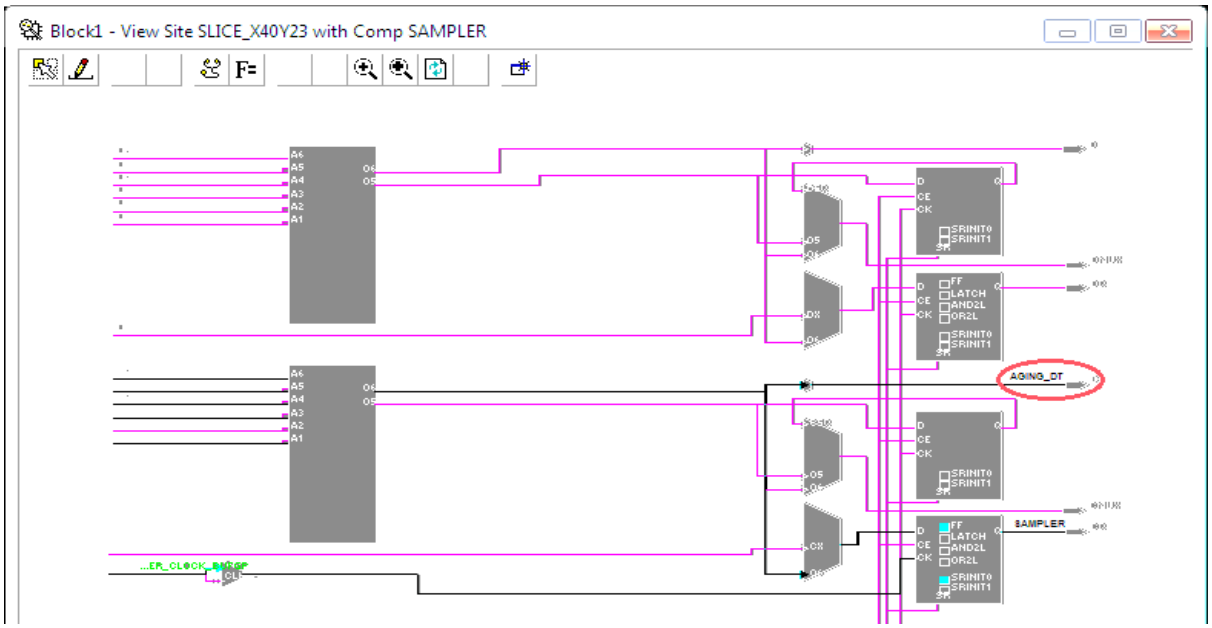

Figure 19. The proposed aging detector can be easily implemented into already existing designs in Xilinx FPGAs

Figure 19 shows an example of the real implementation of the presented solution in a standard design. In the following test and its description, the end of the critical path is named AGING_DT and the final DFF is named SAMPLER.

The proposed solution was tested and validated on Xilinx FPGAs: Digilent's Atlys Spartan FPGA Development board, incorporating a 45 nm Xilinx Spartan®-6 LX45 FPGA device in a 324-pin BGA package on the board, and a single 100MHz clock source[3]. In addition, some tests were done on a ML605[4] board with a 40 nm Virtex-6 device. The boards were connected to a standard PC via USB (JTAG). No any other device or special equipment was utilized or required. The standard ISE Design Suite 13.4 (64bit version) from Xilinx was used. A set of short supporting software for the final data processing was written in GNU C/C++.

Table 2 shows an example of data obtained during the tests. *AGING_DT* column is the sampled aging output, *SAMPLER* is the sampled output of D-Flip-Flop or the output latch, already existing in the original design.

Table 2. An example of the detected risky transitions by the proposed XOR-less aging detector

Address @	AGING_DT @n	SAMPLER @n	AGINT_DT @n-1
n+0	1	1	1
n+1	**0**	**0**	**1**
n+2	0	0	0
n+3	0	0	0
n+4	**1**	**1**	**0**
n+5	1	1	1
n+6	0	1	1
n+7	0	0	0

The key point of the solution is that the CPU has to check only the data consistency of the last two columns – both must be identical. This is fully asynchronous to the CPU performance; the columns must be same at the same memory address location and at any sample time for years; otherwise a delay fault is detected. The data consistency between the *AGING_DT* column at *(n-1)* and at *(n)* position (the first and the third column) should be also kept at any time, naturally only when the logging is off. Data inconsistency may occur very often during asynchronous access of the detector unit and CPU (<1% in our test system). Finally, the table shows two examples of the suspected changes, when the data has changed very close to the clock domain. It is obvious, that the *AGING_DT* signal has changed or was not stable a short time (< 1 ns) close to the previous clock edge [n+0], during 1→0 transition, resp. 0→1 transition in the 2nd case. The parameters of the implemented solution (in the steps set by the used architecture) can be adjusted by special constrains, put on the optimal placement of the utilized BRAM, while only interconnects can be rerouted.

[3] http://www.digilentinc.com/Products/Detail.cfm?Prod=ATLYS

[4] http://www.xilinx.com/products/boards-and-kits/EK-V6-ML605-G.htm

4 Experiments and Results

The main advantage of the experiments described in this chapter is in utilization of the standard tools only and generally available development kits, no other tools or expensive equipment (oscilloscope, logic analyser, etc.) is required at all. The method is based on a simple core design. It is easily scalable thanks to the flexible key part of the design. The design can utilize also programmable internal matrixes for dynamic scaling of the rings.

4.1 65 nm FPGA device and platform

The first test board and the FPGA type used for the first test purposes were Xilinx ML506 board[5] with 65 nm Virtex 5 FPGA XC5VSX50T-FFG1136 manufactured using 65 nm copper CMOS process technology (1.0V core voltage). The device has about 8160 slices, 780 Kb of distributed RAM and 4752 Kb of Block RAM employing 132 blocks, each 36 Kb in each true dual-port RAM block. There is also a socket populated with a 100-MHz oscillator. The programmable clock generator provides 33 MHz, 27 MHz, and a differential 200 MHz clock to the Xilinx FPGA. Please see [*102*], [*103*] and [*104*] for more details about this platform.

4.2 45 nm low-power FPGA device and platform

Regarding 45nm test platform, Digilent's Atlys Spartan FPGA Development board[6] was used for the test purposes, having one Xilinx Spartan®-6 LX45 FPGA on the board, (in my case and FPGA type a chip having approximately 44 K logic cells, 6822 slices with look-up tables (LUT), 54576 flip-flops, 172 pieces of 18 Kb true dual-port RAM blocks of 2088 Kb block memory, etc.). The die is manufactured using a 45nm Samsung low-power copper process technology [*84*] and assembled on the board in a 324-pin BGA package. There is also a single 100 MHz clock source on the board. Please see [*77*] for details about Spartan Xilinx FPGA family and about Atlys board in [*105*].

4.3 40 nm high-performance FPGA device and platform

Some tests were done also on ML605[7] development board utilizing Virtex®-6 XC6VLX240T-1FFG1156 FPGA device manufactured using 40nm process. This device has 241152 logic cells, 37680 slices and 416 pieces of 36 Kb true dual-port RAM blocks (14976 Kb in total in BRAMs only). There is also a differential 200 MHz and a single-ended 66 MHz socketed clock source present on the board. Please see [*78*], [*86*] , [*106*] and [*107*] for more details about this platform.

4.4 28 nm low-power and high-performance FPGA devices and platforms

Two samples of Digilent's low-cost ZedBoard™ Field Programmable Gate Array (FPGA) Development board[8] were used for the test and measurement purposes, having one Xilinx Zynq™-7000 SoC (All Programmable System on Chip) FPGA type XC7Z020-1CLG484 on the board. The FPGA device is a member of the Artix™-7 low-cost Xilinx FPGA product family, intended for the application segment similar to previous Spartan© product families (see Xilinx press release from July 17, 2012). The die is manufactured using TSMC's advanced

[5] http://www.xilinx.com/products/boards-and-kits/HW-V5-ML506-UNI-G.htm

[6] http://www.digilentinc.com/Products/Detail.cfm?Prod=ATLYS

[7] http://www.xilinx.com/products/boards-and-kits/EK-V6-ML605-G.htm

[8] http://www.digilentinc.com/Products/Detail.cfm?Prod=ZEDBOARD

28 nm high-performance, low-power copper process technology, incorporating dual-core ARM® Cortex™-A9 based application processor unit (APU), programmable logic (in my case an FPGA type having approximately 85 K logic cells, 53200 look-up tables (LUT), 106400 flip-flops, 140 pieces of 36 Kb true dual-port RAM blocks of 560 KB block memory, etc.), cache or other memories, interfaces, DSP blocks, etc. Please see e.g. Xilinx datasheets [*79*], [*108*], [*87*] and [*109*] for more details about the FPGA families, including all the detailed information mentioned in the WP423 in [*110*]. The Kintex family details can be found in [*88*]. The FPGA is assembled on the board in a 484-pin BGA package. There is also a single 100 MHz clock source available on the board. Please see [*111*] and [*112*] for more details, as well as the ZedBoard community web [*113*] for additional information and support.

4.5 Software Tools Used

Only a standard software set of tools from Xilinx, ISE Design Suite 14.x in the 64bit version was used. The proprietary data processing software was written in GNU C. This my new software pack is a part of a new Open-Source data processing toolbox, used especially for devices parameter measurement, mapping, optimum parameter-aware placement and routing, up to a final project testing and reliability assessment purposes.

4.6 Selected results

The following figures show a short set of selected results. The first figure 20 shows an example of results of my measurements in this area, results of measurements of internal FPGA delays (look-up tables - LUT - plus latch delay, *An* input to *DQ* output, plus interconnects - NET). It is based on evaluation of the output frequency of each ring oscillator using the absolute method presented in this document. It shows measurable and clearly detectable mutual impact and changes in ring oscillator frequency and delays in the logic, if selected set of oscillators is switched on and off. Ring #30 has visible immediate impact to frequency (delays) of ring #31. Ring #17 influences ring #30 in much lower way. Ring #1 is located completely out of the previous set of ring oscillators. This ring is obviously not significantly affected by work mode or workload of any other ring oscillator. The following figures show a comparison of both 28 nm and 45 nm low-power platforms for the overall design power consumption, however measured only at the core voltage power rails (V_{core} or V_{int}). One important fact has to be noted here, that the core voltage rail is not routed only to the FPGA device (please see the schematic diagram and other related documents), but also to one external device. Based on the modifications made to one board (the external devices were physically disconnected from the power rails), the measurement error caused by the mentioned fact was evaluated below 12 % of the total values. This is considered to be not significantly affecting the data and results presented in this document. The experiments were performed on 2 pieces of the boards for each technology (4 development boards in total) with measured differences below acceptable 10 % overall error. Our 28nm Zynq device is clearly more sensitive to voltage variations than the previous Spartan 45nm technology node. Figire 30 shows obvious issues in 28 nm devices caused by the internal protected mechanism and XADC unit. Figure 31-33 show an example of the measured aging waveforms and the last figure shows a proof of the methodology and that all ring oscillators behave the same way within the selected sets or groups of oscillators, it means the group, where the rings are oscillating all the time, and the two other groups where the rings are held at zero or one logic levels for very long time (typically 1 hour) in order to stress the entire path and transistors in the logic path, and the oscillations are enabled only for a short time of 1 ms in order to measure the performance of the chain, transistors and units.

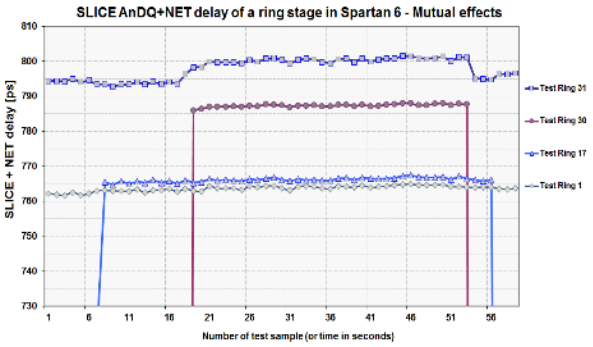

Figure 20. Example of mutual impact and crosstalk and the temperature impact on delays in selected SLICEs and ring oscillators.

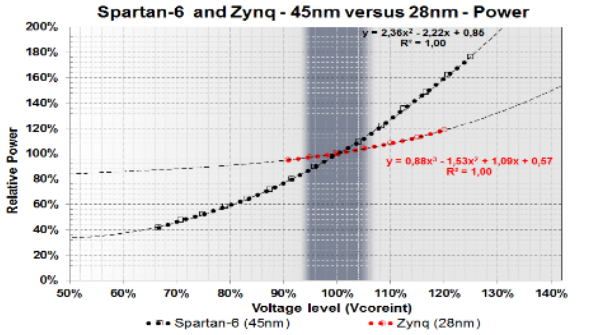

Figure 21. Comparison of both platforms for the overall design power consumption (relative measures).

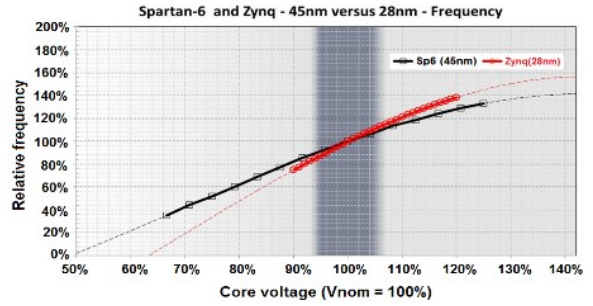

Figure 22. Comparison of both platforms for maximum working frequency with respect to the core voltage (the area in grey indicates the recommended working range by the FPGA

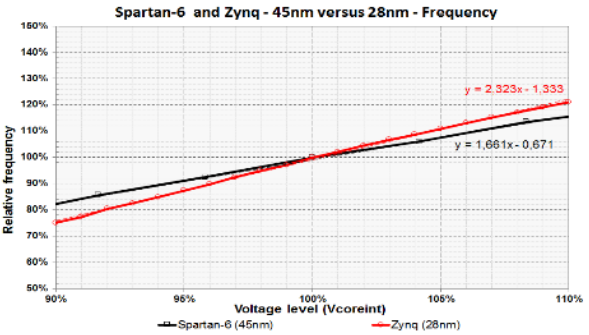

Figure 23. Comparison of both platforms with respect to the recommended working conditions in Xilinx specifications.

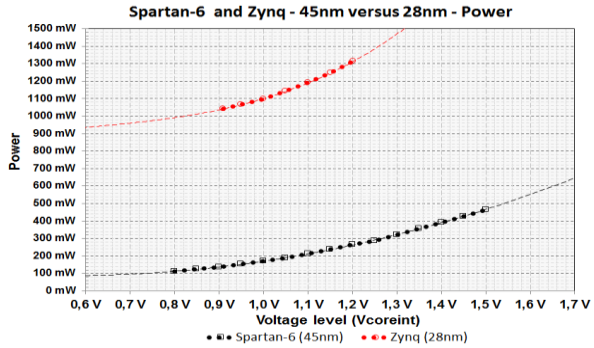

Figure 24. Comparison of both platforms for overall design power consumption.

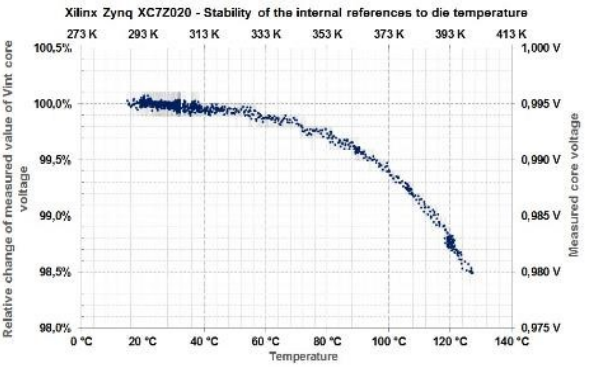

Figure 25. An example of leakage measured in one of our previous temperature-related experiments.

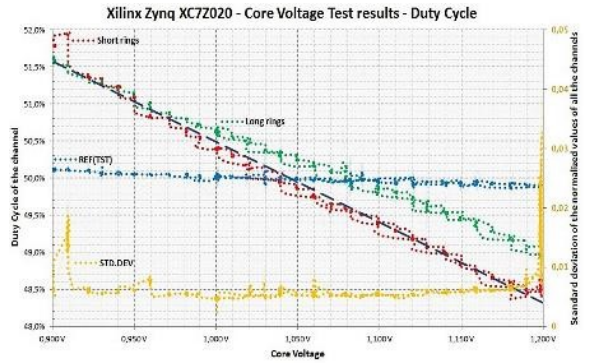

Figure 26. Duty cycle and detailed core voltage change results for 28 nm Zynq device.

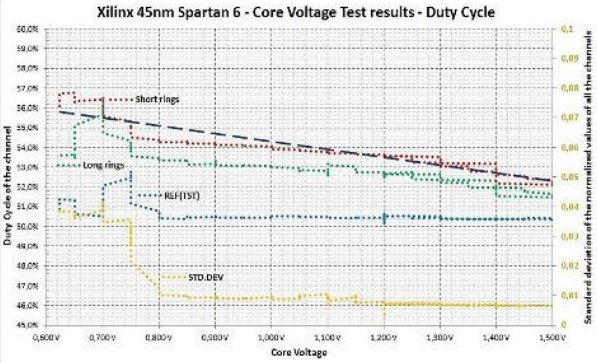

Figure 27. Measurement results of the duty cycle to core voltage change for 45 nm Spartan 6.

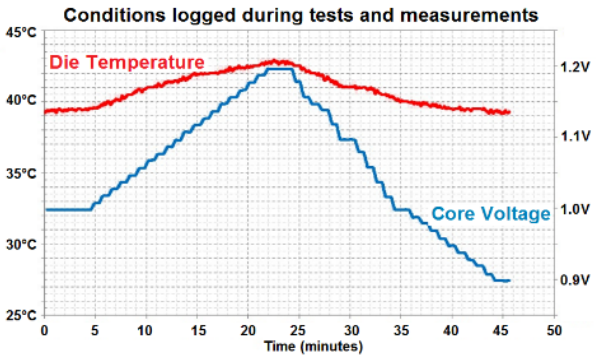

Figure 28. An example of the log data during the measurements and experiments.

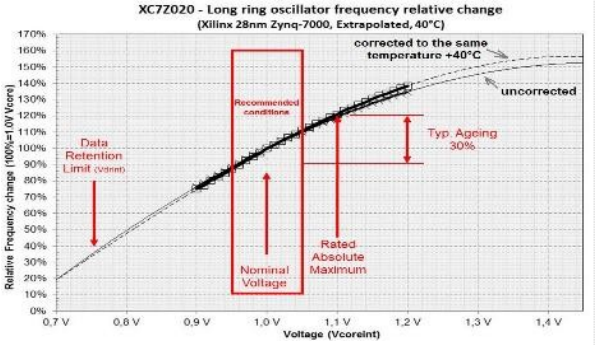

Figure 29. The maximum frequency relative change and key space available for mitigation of aging effects.

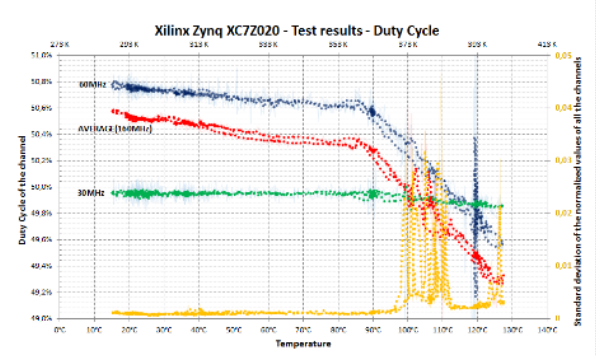

Figure 30. Duty cycle of ring oscillators with various lengths to the die temperature measured by BRAMs.

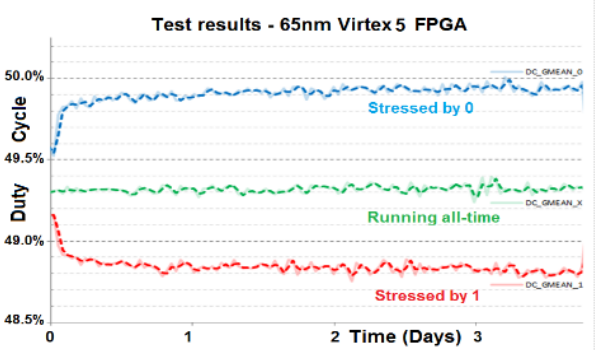

Figure 31. An example of the application of the reliability lab-on-chip methodology - BTI in 65nm FPGA with V_{th} changes projected to duty cycle.

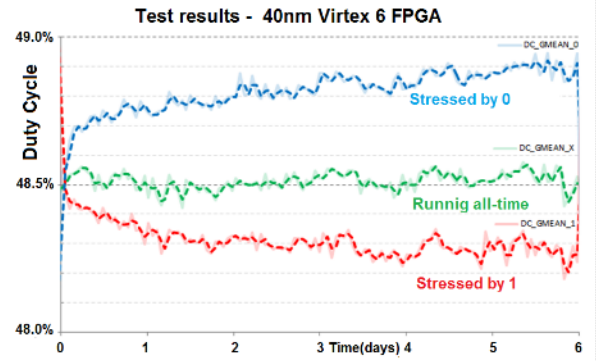

Figure 32. An example of degradation processes measured in 40 nm technology – change in the duty cycle.

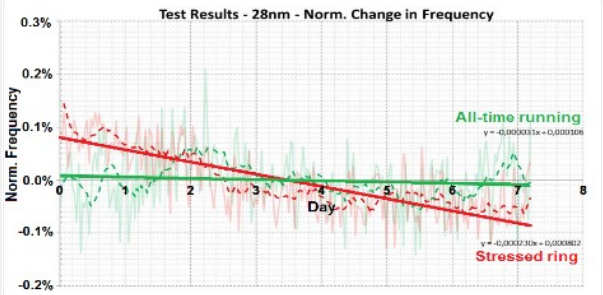

Figure 33. An example of degradation processes measured in high-performance 28 nm Virtex technology, showing relative frequency of ring oscillators working in different modes.

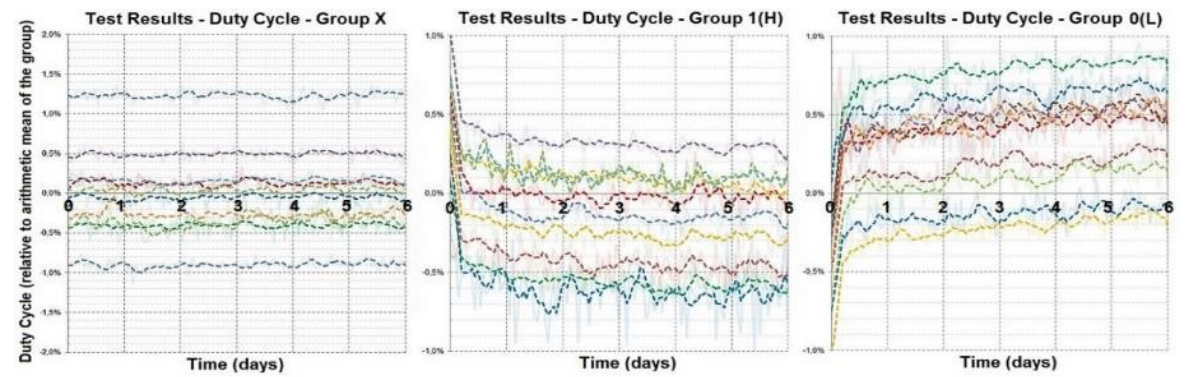

Figure 34. An example of unrolled results of members of the measured groups of ring oscillators – all rings in the group behave in the same way.

5 Summary, conclusions, discussion and open questions

I have presented a new methodology and its key theory background. The reconfigurable lab-on-chip concept is available as well, including the underlying method and selected results from in-situ measurements, based on undersampling and on-chip generated and analysed BRAM data streams. The method allows extremely easy and precise way of measurement of parameters and parameter shifts in devices and circuits, reliability testing, better estimation of reliability parameters and their initial or periodic assessment. Is also includes all the developed multi-platform solutions, new equations, XOR-less aging detection unit and also the key differential aging measurement mode using BRAMs. A lot of new, sometimes also previously unpublished data and results from measurements and experiments on various technologies down to very popular 28 nm were included and discussed as well. The area of research itself seems to be also a new one. For example Google Scholar webpage shows, when looking for the search results of the keywords "FPGA, aging, undersampling", the obvious exclusivity of the research presented in this document, that it is obviously unique in its topic as well as results, volume and set of activities. It is also very difficult to find any other paper dealing with BRAM utilization for the purpose and in the way presented in this document.

The presented results show and also confirm generally observed important trends in microelectronics and the modern nanotechnologies. The method is applicable to general as well as complex systems. I have implemented and validated the method and trends on complex systems. The presented solution enables additional reliability enhancements with extremely low added costs, positively affecting the design's final MTBF (Mean Time Between Failures) or MTTF (Mean Time To Failure) reliability parameters.

The presented work and methodology is definitely based on modern solutions and technologies. The results shown in this document validates the required and sufficient sensitivity and easy implement ability in modern systems and measurement of various parameters of circuits and devices. However the experiment and measurements were not performed on larger amount of various products and pieces of FPGA devices, chips and programmable circuits. In the microelectronic industry, 50 to 200 pieces are typically used for general information and technology qualification, Intel has presented a data from millions of pieces shipped to customers. Any such a volume is not reachable at all in our conditions. At our university, we have a possibility to test one piece only, or a few pieces from approximately 10 boards used for teaching purposes. However, it is not possible to make any piece unusable for students and teaching processes, damage it, or lose the warranty in case of the very new development boards and other products. Therefore, it is intended to apply the presented methodology and implement such solutions in higher volumes and systems and we are focusing on closer cooperation with our existing or new partners.

The future is intended for detailed study of the already implemented as well as many new solutions and mechanism, their analyses, description, modelling, and better understanding. Our growing reliability data bank is an important part of the final methodology and toolbox, allowing complete measurement of most of the today's internal structures, their usage for special parameter-aware placement and routing in critical designs, evaluation or estimation of the key reliability parameters with respect to the initial values or points, up to the key simple or complex continuous or on-demand reliability assessments tasks.

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7 List of Publications and Presentations of the Author

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